MODEL 2760

UNIVERSAL SIGNALING ANALYZER MAINFRAME

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CONTENTS

MODEL 2760

UNIVERSAL SIGNALING ANALYZER

MAINFRAME

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1. GENERAL

A. Scope

1.01 This publication provides a complete description of the Model 2760 Universal Signaling Analyzer mainframe assembly and its Resident Module. Information on its use and applications is included. Limited information on various plug-in modules is also included.

1.02 This practice is being reissued to make minor corrections. The bulk of this issue is substantially the same as the previous issue. For minor corrections the issue numbers included in page headings are only changed for those pages actually affected by the new issue; therefore, the issue number on each page indicates the most recent change to that page. The page(s) affected by this new issue is/are the cover and pages 1, 4, 99, 111, and 112.

B. Organization

1.03 The information contained in this publication is organized as follows:

(a) PART 1. GENERAL: Contains information on the scope and organization of this publication and on the Model 2760 specific applications.

(b) PART 2. INSTALLATION: Furnishes general installation instructions including unpacking, inspection, mounting procedures, interconnections, power and ground connections, and internal switch settings for the Model 2760 mainframe assembly.

(c) PART 3. DESCRIPTION: Provides a basic description of the Model 2760 physical characteristics, front and rear panel layout, displays, switches, indicators, keypad, Resident Module, and plug-in modules.

(d) PART 4. OPERATION: Presents detailed information on how to set up and operate Model 2760. Information is included on test connections, programming, display interpretation, signaling parameters, and plug-in module selection, etc.

(e) PART 5. THEORY OF OPERATION: Contains specific details on the theory of operation and circuit descriptions of the Model 2760 mainframe assembly.

(f) PART 6. MAINTENANCE: This section provides maintenance and alignment information for the mainframe assembly.

(g) PART 7. DIAGRAMS: This section contains functional diagrams, parts location diagrams, and schematic diagrams for the Model 2760 mainframe assembly.

(h) PART 8. ELECTRONIC PARTS LIST: Furnishes a list of all electronic parts used in the Model 2760 mainframe assembly.

(i) PART 9. GLOSSARY: Defines the terms, abbreviations, and symbols used in this publication.

C. Applications

1.04 The Model 2760 Universal Signaling Analyzer is a powerful tool for testing in-service circuits, diagnosing signaling problems, and locating the source of trouble. It may also be used for testing new circuits (not yet in-service) to insure signaling limits are met.

1.05 The unit's high impedance inputs may be bridged on a circuit at any point. All register (address) and line (supervision) signaling sequences on that circuit are captured and may be displayed for review.

1.06 Maintenance Testing and Troubleshooting

1.07 The Model 2760 automatically detects frequency component errors in all MF signaling systems, plus element (bit) errors and other faults in the CCITT No. 4 system. These errors are displayed as a dash (-) inserted at the appropriate position(s) in the signaling sequence. The MF plug-in module being used will indicate the actual MF frequencies (tones) received for signals displayed as a dash (-).

1.08 Interpretation of the error positions often immediately pinpoints the trouble to a specific telephone office along a circuit. The office may be a local, regional, gateway, transit, terminal, or other exchange.

1.09 Other error indications are provided to detect signals violating previously programmed limits for no tone gap, pulse width, and received signal level. This information is very useful for:

(a) Diagnosing problems caused by short-pulsing or erratic senders, faulty repeaters, slow echo suppressors, and other similar equipment which affects timing parameters.

(b) Diagnosing problems caused by marginal sender output level, faulty transmission, and other level-affecting conditions.

(c) Checking circuits to the margin limits of their tone receiver detection sensitivities.

1.10 For many MF signaling systems the Model 2760 is capable of displaying the actual measured values of the timing and level parameters for each digit-code.

1.11 The Model 2760's dual row display (A and B) together with its sequence comparison capabilities allows simple checks on the accuracy of signaling repeaters, translators, and converters. Equipment such as DP to MF converters, DP repeaters, Loop to E&M converters etc. is easily checked. If the output of such equipment is not a faithful reproduction of the input it is immediately apparent on the dual display. An alarm indication may also be provided.

1.12 Service Observation

1.13 The Model 2760 may also be used for monitoring call completions and gathering the data necessary to evaluate and improve the call completion rate. It automatically captures all register (address) and line (supervision) signaling information for each call. It also provides an audio output for determination of a call's final disposition, e.g. busy, reorder, ring/no answer, abandoned, etc.

1.14 Use of the programmed sequence recognition feature enables selective recording/monitoring of traffic to specific countries, areas, or subscriber lines.

1.15 The optional 2760-21 Printer Control Module has many data storage and analysis features especially useful for service observations activities.

1.16 Fraudulent and Malicious Call Monitoring

1.17 The ability to program signaling sequences for automatic comparison to live or recorded traffic permits detection of fraudulent and malicious calls. When a dialed number match is detected, the Model 2760 initiates an alarm condition and captures all the register (address) and line (supervision) signaling information in memory for later review. The alarm output may be used to activate a recorder.

2. INSTALLATION

2.01 This part contains information needed to connect and install the Model 2760 mainframe assembly. This information includes:

- Initial inspection
- Mounting procedure
- Interconnections
- Power and ground connections
- Internal switch settings.

A. Initial Inspection

2.02 The 2760 is carefully inspected, both mechanically and electrically, before shipment. It should be working properly when received. If damage from transit is found, notify the transportation carrier immediately.

B. Mounting Procedure

2.03 The 2760 may be rack mounted or used as a portable unit. In either case, provide clearance for air inlets and outlets to ensure proper cooling.

Warning: All module receptacle slots in the 2760 must be covered with dress panels or equipped with plug-in modules to ensure proper air flow.

2.04 Portable Operation

2.05 Place the 2760 on a convenient table, work bench, mobile cart, or on top of other related equipment. Provide air flow clearance for cooling all equipment.

2.06 Rack Mounting

2.07 The 2760 is shipped with two rack mounting brackets packaged separately. The brackets can be used to mount the 2760 either in a 19- or 23-inch rack. Also, the 2760 can be "flush" or "five-forward" mounted. To "flush" mount in a 23-inch rack do ONLY steps (7) and (15) listed below.

Danger: Electrical shock hazard. Make sure the 2760's AC power cord is unplugged before performing any of the steps listed below.

2.08 To install the brackets:

(1) Remove the Resident Module from the 2760.

(a) On the Resident Module front panel, loosen and remove the four screws and washer securing the Resident Module to the 2760.

(b) Pull out the Resident Module part way to expose the main input board.

(c) Disconnect the plug from jack J13 on the jack board. (See Fig. 30).

(d) Disconnect the plugs from jacks J1, J2, and J3 on the main input board. (See Fig. 32).

(e) Set the Resident Module aside.

(2) Remove the dress panels (or plug-in modules) from the two farthest right-hand plug-in slots. Pull on black knob at bottom of panel or module.

(3) Remove bottom cover.

(a) Place 2760 upside down.

(b) Loosen and remove four sets of screws and washers securing cover to the 2760 chassis.

(c) Lift cover up and out.

(4) Loosen fan housing assembly.

(a) Loosen and remove five flathead screws securing the fan housing assembly to 2760 chassis.

(b) Pull fan housing upward to provide free access to the bolt securing the handle.

(5) Loosen and remove the bolts and washers securing the handles to the 2760.

Note: Two sets of threaded inserts are available on the 2760, one set near the front of the 2760 for "flush" mounting and another set near the center of the 2760 for "five-forward" mounting.

(6) Secure the bolts and washers on the handles for safekeeping. Store handles for future use.

(7) Secure a rack mounting bracket to the threaded inserts on each side of the 2760 with 10-32 flathead screws.

(8) Resecure fan housing assembly.

(9) Replace bottom cover.

(10) Place the 2760 right-side up.

(11) Replace all removed dress panels (or plug-in modules).

Note: To insure proper placement of a plug-in module, carefully slide the module into the mainframe assembly, then apply thumb pressure at a point slightly above and to the right of the module's plastic plunger. Complete the insertion by depressing the plastic plunger into its locked position. Refer to Fig. 1.

(12) Reconnect the plugs to jacks J1, J2, and J3 on the main input board of the Resident Module.

(13) Reconnect the plug to jack J13 on the jack board of the Resident Module.

(14) Replace and secure the Resident Module inside the 2760.

(15) Mount the 2760 in the rack.

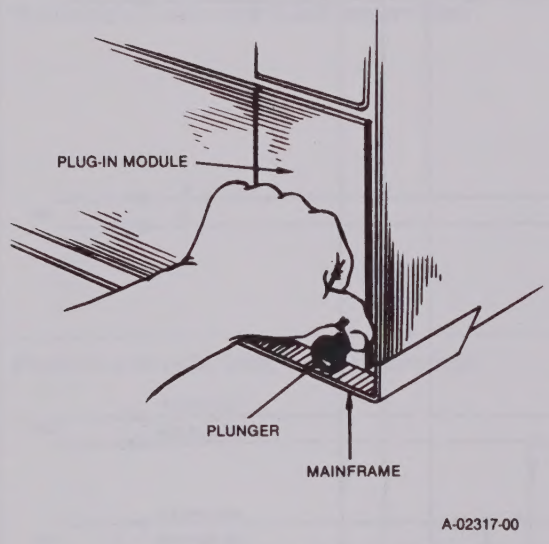


Fig. 1—Plug-In Module Insertion

C. Interconnections

2.09 The 2760 can be connected to circuits under test in a variety of ways. Connections can be made to front panel jacks or to barrier strip terminals at the rear of the 2760. Fig. 2 illustrates the interconnections between the Resident Module front panel jacks and the barrier strip terminals. Table A lists the circuit test connection options for several types of circuits to be monitored. Refer to Part 3 for descriptions of the other front panel jacks.

D. Power and Ground Connections

2.10 The 2760 can be powered from a source supplying 105 to 125 Vac or 210 to 250 Vac, 47 Hz to 63 Hz. Always verify what primary ac voltage the 2760 is set for by observing the 115/230 switch located on the rear panel of the 2760.

Warning: If the 2760 is not set for the proper voltage, or is not properly fused, it may be seriously damaged.

2.11 If it is necessary to change the primary voltage, perform the following steps.

(1) Ensure that the 2760 is disconnected from the external power source and that the POWER switch is OFF.

(2) Slide the 115/230 switch on at the rear panel of the 2760 to the required primary ac voltage.

(3) Check to ensure that you are using the proper size fuse. A 2A slow-blow fuse is required for 115 Vac line operation. A 1A slow-blow fuse must be used for 230 Vac line operation.

2.12 To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the 2760 front panel and cabinet be grounded. The 2760 is equipped with a three-conductor power cord which, when plugged into a properly grounded receptacle, grounds the 2760. A binding post, located on the rear panel, allows connection of the 2760 directly to central office ground.

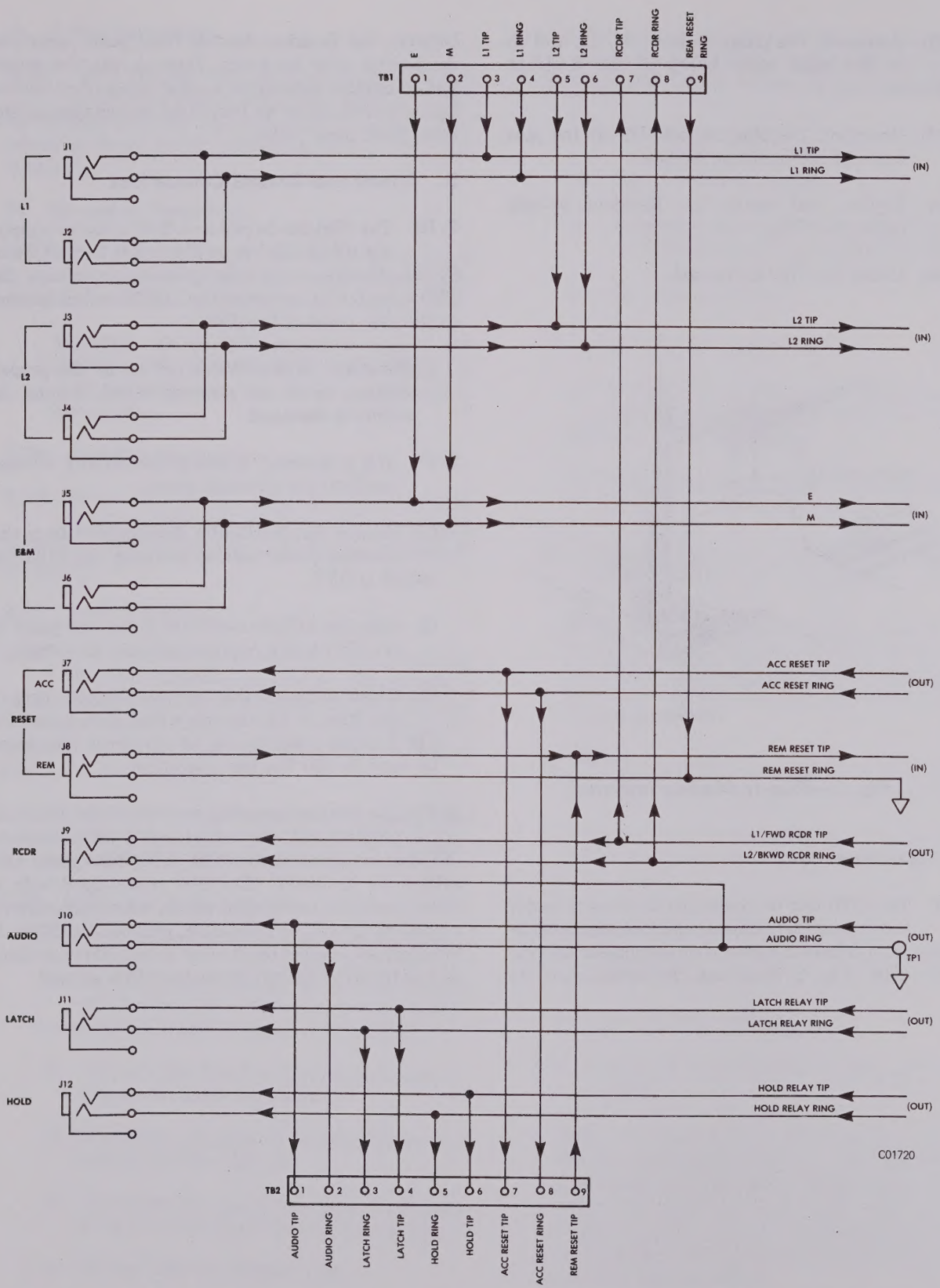


Fig. 2—Resident Module Jacks and Barrier Strip Terminal Interconnections

TABLE A

CIRCUIT TEST CONNECTIONS

CIRCUIT TYPE	CONNECTIONS
Loop circuits with sleeve lead supervision	(1a) L1 jack J1 or J2 or tip on TB1-3 and ring on TB1-4. or (1b) L2 jack J3 or J4 or tip on TB1-5 and ring on TB1-6.
Two-wire circuits with E&M supervision	(1a) L1 jack J1 or J2, or tip on TB1-3 and ring on TB1-4. or (1b) L2 jack J3 or J4, or tip on TB1-5 and ring on TB1-6. and (2) E&M jack J5 or J6 (E lead on tip, M lead on ring) or E lead on TB1-1 and M lead on TB1-2.
Four-wire circuits with E&M supervision	(1a) Receive pair on L1 jack J1 or J2, or tip on TB1-3 and ring on TB1-4. (2a) Transmit pair on L2 jack J3 or J4, or tip on TB1-5 and ring on TB1-6. or (1b) Receive pair on L2 jack J3 or J4, or tip on TB1-5 and ring on TB1-6. (2b) Transmit pair on L1 jack J1 or J2, or tip on TB1-3 and ring on TB1-4. and (3) E&M jack J5 or J6 (E lead on tip, M lead on ring) or E lead on TB1-1 and M lead on TB1-2.
Note: See Fig. 2 for jack and terminal interconnections.	

E. Internal Switch Settings

2.13 The 2760 will detect a reverse battery condition on both L1 and L2 input ports. E&M lead on-hook and off-hook conditions are also detected. Four switches inside the Resident Module determine how the 2760 interprets reverse battery and E&M lead conditions. The switches (S1-S4) are located on the Main Input Board (See Fig. 3).

2.14 Switches S1 and S2 control the line (supervision) signaling, reverse battery detection for L1 and L2 input ports respectively. Switch S3 controls the on-/off-hook states of the E lead input port. Switch S4 controls the on-/off-hook states for the M-lead input port.

2.15 It is important to note that switches S1 and S2 cause a tip/ring turn-over for L1 and L2 respectively (See Fig. 3). Table B summarizes the reverse

battery conditions for the Normal and Reverse settings of S1 and S2 switches.

2.16 Switches S3 and S4 each consist of a group of 2 switches designated C1 and C2 (See Fig. 3). Table C summarizes the E&M lead conditions for the various settings of S3 and S4 (See Fig. 33).

2.17 Internal switches S1 and S2 are factory set at "normal"; switch C1 for both S3 and S4 is factory set at "off"; and switch C2 for both S3 and S4 is factory set at "on". Therefore, the 2760 normally considers a line reversed when the ring lead is more positive than the tip lead by at least 2V. Similarly, the 2760 normally considers an E-lead more positive than −7 V to be off-hook, and an M-lead with an open circuit is considered to be on-hook.

2.18 Should an office require different criteria for reverse battery detection and/or for E&M on-/off-hook detection, then the internal switches may easily be set as required. To set the internal switches:

(1) Ensure that the 2760 is not powered up and disconnect power cord.

(2) On the Resident Module front panel, loosen and remove the screws and washers securing the Resident Module to the 2760.

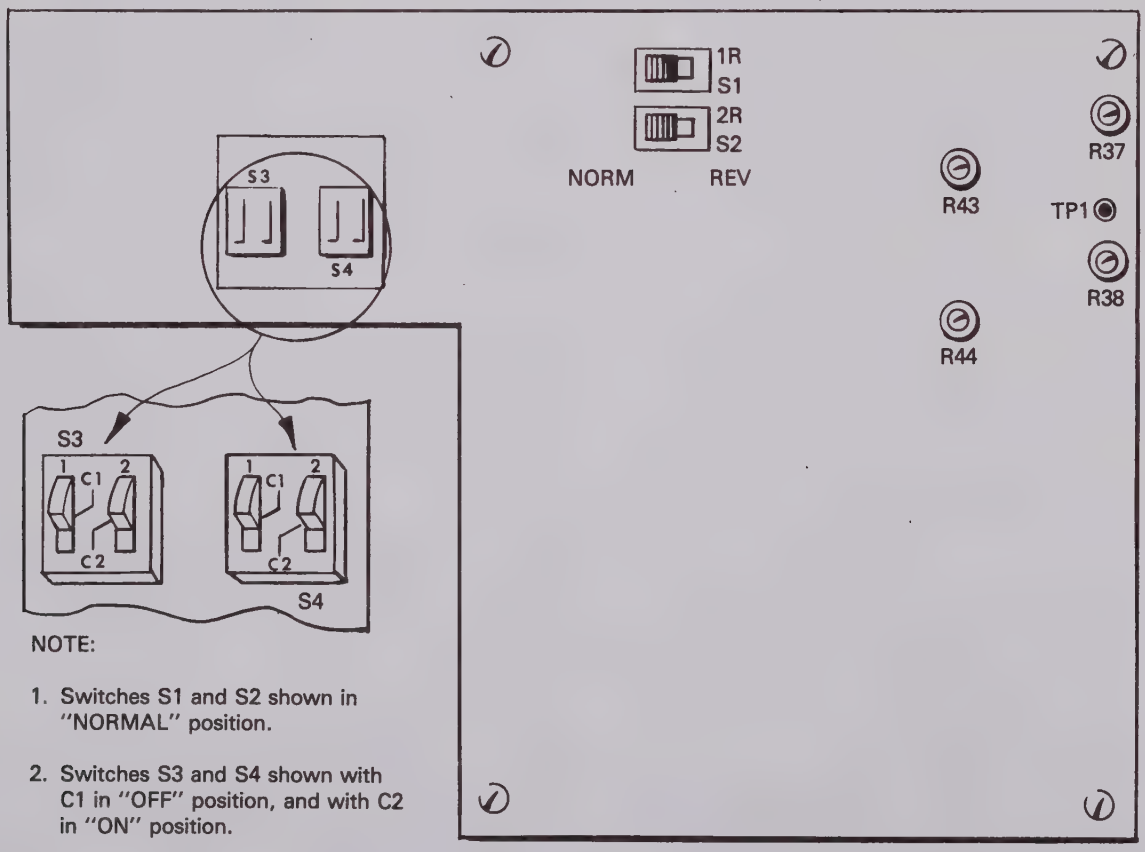
(3) Pull out the Resident Module to expose the main input board.

(4) Set the internal switches as needed (See Fig. 2, Table B, and Table C).

(5) Replace and secure the Resident Module.

(6) Reconnect power cord and apply power to the 2760.

(7) Verify that the 2760 is correctly detecting reverse battery and/or E&M on-/off-hook conditions.



NOTE:

1. Switches S1 and S2 shown in "NORMAL" position.
2. Switches S3 and S4 shown with C1 in "OFF" position, and with C2 in "ON" position.
3. A "1" or "2" marks the "ON" positions of C1 and C2; the "OFF" positions are unmarked.

Fig. 3—Main Input Board Switches for Reverse Battery and E&M Lead Conditioning

TABLE B

REVERSE BATTERY CONDITIONS

INPUT PORT	SWITCH POSITION	DETECTION CRITERIA
L1	S1 at "normal"	Ring lead more positive than the tip lead by at least 2 V.
L1	S1 at "reverse"	Tip lead more positive than the ring lead by at least 2 V.
L2	S2 at "normal"	Ring lead more positive than the tip lead by at least 2 V.
L2	S2 at "reverse"	Tip lead more positive than the ring lead by at least 2 V.

TABLE C

E&M LEAD CONDITIONS

SWITCH POSITIONS		OFF HOOK		ON HOOK	
C1	C2	CONDITIONS	SWITCHING POINT	CONDITIONS	SWITCHING POINT
SWITCH S3		E-LEAD			
OFF	ON	GROUND	> −7 V	BATTERY, OPEN	< −8 V
OFF	OFF	BATTERY	< −8 V	GROUND	> −7 V
ON	ON	GROUND	> −19 V	BATTERY	< −20 V
ON	OFF	BATTERY	< −20 V	GROUND, OPEN	> −19 V
SWITCH S4		M-LEAD			
OFF	ON	BATTERY	< −20 V	GROUND, OPEN	> −29 V
OFF	OFF	GROUND	> −19 V	BATTERY	< −20 V
ON	ON	BATTERY	< −8 V	GROUND	> −7 V
ON	OFF	GROUND	> −7 V	BATTERY, OPEN	< −8 V

3. DESCRIPTION

A. GENERAL

3.01 The Model 2760 is an intelligent signaling analyzer with many advanced features for monitoring the register (address) and line (supervision) signaling information present in live (or recorded) telephone traffic. A fully modular design allows the instrument to economically handle many different signaling and supervision systems in use around the world.

3.02 The intelligence needed for such application versatility is provided by a microprocessor in the instrument's mainframe. Modular plug-ins are used (as required to handle the different signaling and supervision systems to be monitored).

3.03 Plug-ins are available for such systems as:

- R2/MFC, MF2, and MF3
- E&M or Loop DP (both British and North American types)
- AC9 and AC11 (British)
- CCITT #3 register and line signaling
- CCITT #5 register and line signaling
- DTMF (MF4 Touch Tone®)
- North American MF (R1 address signaling)
- North American 2600-Hz SF pulsing and supervision (R1 line signaling).

3.04 The instrument can be bridged anywhere on 2-wire, 4-wire, or 6-wire circuits without disturbing normal service. It recognizes all address digit/code signaling (register signaling) and supervision/control events (line signaling) appearing on a circuit.

3.05 Information Capture and Display

3.06 Signaling and supervision information monitored by the Model 2760 is displayed in real time as received and is also stored in memory for later review by recall to the displays.

3.07 Register signaling digits and codes are presented on a dual (two row) display which allows simultaneous, separate viewing of both forward and backward sequences on R2, MFC, MF2, and CCITT #4 circuits. The displays show an exact sequence of events.

3.08 The dual display also permits easy, one-for-one digit comparisons between the inputs and outputs of repeaters, translators, and similar equipment used in various signaling arrangements.

3.09 Up to 16 digits/codes can be shown on each row of the dual display. Even the longest signaling sequences, up to 240 digits/codes per call, may be captured in memory for each row of the display. The full sequence of digits/codes captured for a call may be easily reviewed by scanning forward or backward across the dual display at the press of a button.

3.10 The Model 2760 can be instructed to either:

- Store digits/codes for only a single call by automatically erasing from memory all previously stored digits/codes when a new seizure occurs, or
- Store digits/codes for multiple calls until its 240-character memory is filled.

The latter mode allows easy comparison of register signaling events from one call to the next.

3.11 All supervision (line signaling) events occurring during a call are also captured in memory for later recall to the unit's row A display. The instrument can store up to 15 supervision events per call. In addition, the following events are displayed in real time by panel indicators:

- Seizure
- Answer
- Clear Forward
- Clear Back
- Release
- Blocked (Busy).

3.12 Other LED indicators show the exact status of circuit leads during the time that a call is being monitored. Depending on the type of circuit, these indications may include loop off-hook and line polarity reversal as well as E&M lead conditions.

3.13 As each digit/code or supervisory signal is received, the Model 2760 examines it for error conditions. Depending on the type of signaling/supervision being monitored, the error checking may include:

- Minimum/maximum tone duration, pulse width, no-tone gap, forward/backward delay, and other timing parameters
- Minimum/maximum acceptable tone levels
- Presence of two, and only two MF tones per digit
- Certain other parameters.

3.14 The instrument displays a dash (-) at the appropriate position in the signaling sequence for invalid MF signals not composed of two, and only two tones. Similarly, a dash is displayed for invalid CCITT #4 digits/codes not composed of four, and only four elements (bits). When monitoring CCITT #4 line signaling, a dash indicates certain invalid supervisory signals.

3.15 For error conditions indicated by a dash, the Model 2760 will either:

- Produce an alarm output and freeze all call data in memory, or
- Continue monitoring other calls, depending on programming.

3.16 For many signaling systems, the instrument can be instructed to include numerical error codes in the display of register/supervisory signals violating programmed limits for (a) no-tone gap, (b) pulse width, and (c) received level. Other error codes are provided to indicate frequencies received for invalid signals displayed as a dash.

3.17 The unit can also display actual measured values of a, b, and c above for signaling digits and codes. All information is displayed in real time as detected, and is recallable from memory by scanning with the cursor controls.

3.18 Recognition of Signaling/Supervisory Event Sequences

3.19 Up to 10 sequences, having up to 16 events each, can be preprogrammed via keypad for automatic comparison with calls being monitored. Events can be either register signaling digits and codes or supervisory signals.

3.20 When comparing stored sequences with live traffic the analyzer checks for either a match or a mismatch, depending on programming. If the condition of interest exists, alarm contacts close and all information is held in memory for recall to the displays. Programming also allows:

- Comparing the stored sequence with only a portion of the received sequence (involves entering universal match "wild card" characters)
- Comparing some or all of the register signaling events shown on the row A display with some or all of those shown on row B.

3.21 These flexible sequence recognition features make the 2760 a powerful tool for:

- Detecting signaling conversion/translation errors
- Checking the operation of pulsing repeaters and correctors
- Finding supervisory faults that lead to billing errors
- Selectively recording traffic to specific countries, areas, or subscribers
- Monitoring fraudulent and malicious calls.

3.22 Additional Features

3.23 Other features of the Model 2760 include:

- Audio monitor speaker
- Error and sequence match alarm (contact closure) outputs
- Outputs for driving a hard-copy printer or strip chart recorder
- Remote reset inputs and outputs for control by and of other external equipment
- Time-of-day clock.

B. Physical Description

3.24 The Model 2760 Universal Signaling Analyzer is a portable instrument weighing approximately 25 pounds (11.3 kg) and measuring 10.5 inches (27.6 cm) high, 17.0 inches (43.2 cm) wide, and 12.0 inches (30.5 cm) deep. The housing is fabricated of AST aluminum alloy. The housing exterior is spray painted with a green wrinkle finish. A 2 position wire bail mounted on the bottom of the housing is designed to serve as a tilt stand for easy viewing. U-shaped 2 position side handles are also provided for easy carrying. Brackets are supplied for mounting in 19- (48.3 cm) or 23-inch (58.4 cm) racks.

C. Front Panel

3.25 The Model 2760 front panel switches, indicators, displays, and keypad are shown in Fig. 4.

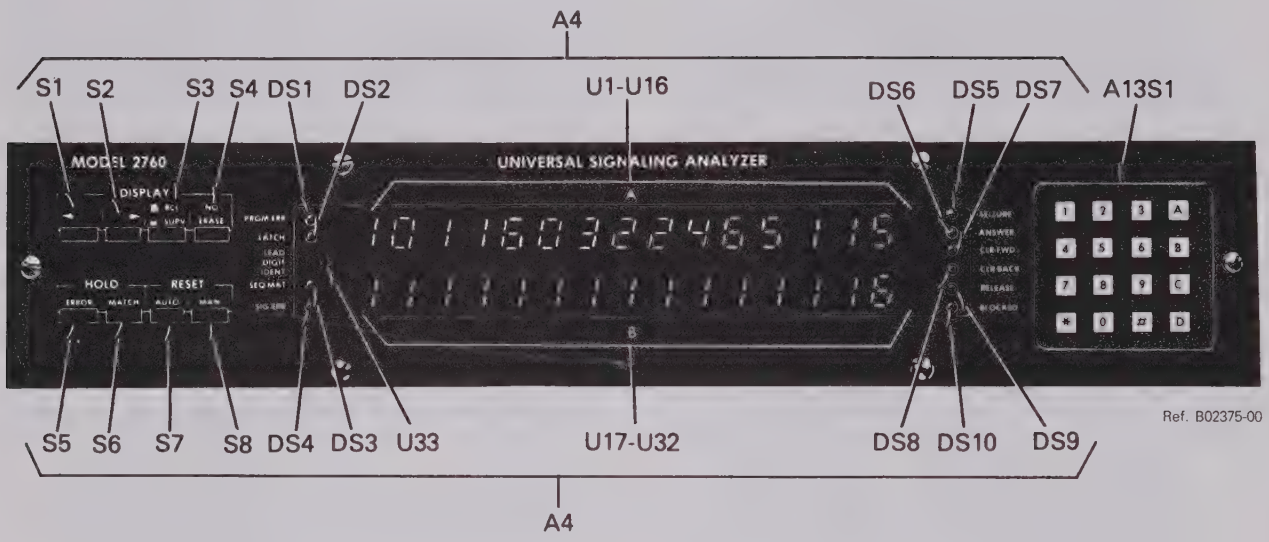


Fig. 4—Front Panel

D. Displays

3.26 DISPLAY A: Display is a 16 character (alphanumeric), 7 segment plus decimal point per character LED display with a 0.5 inch character height. (See Fig. 5.)

3.27 DISPLAY B: Display is a 16 character (alphanumeric), 7 segment plus decimal point per character LED display with a 0.5 inch character height. (See Fig. 5.)

3.28 All 32 LED readout devices are mounted in an inverted position so the decimal point appears as a dot above and to the left of each digit. When lighted, the dot signifies 10 is to be added to the digit displayed. In this way the numbers 11-20 may be represented by a single LED readout device (dot lighted) as well as 0-9. (See Fig. 5.)

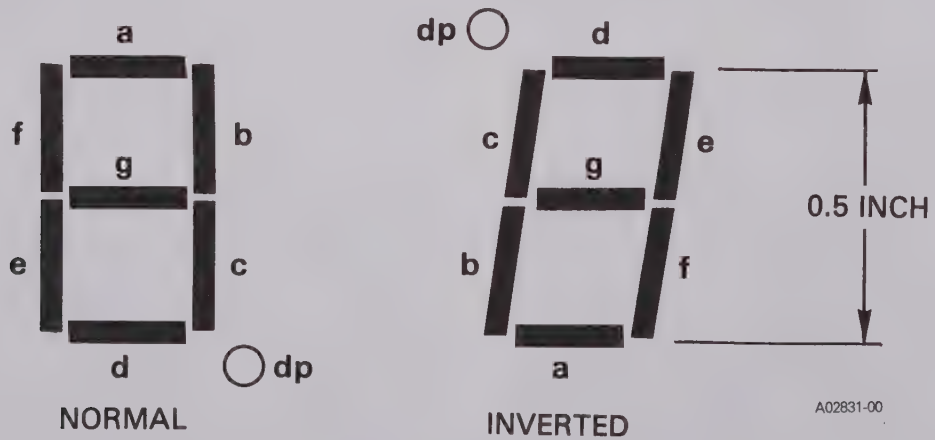


Fig. 5—Seven Segment Readout Device

3.29 Display Modes

3.30 The dual DISPLAYS A and B are used in three different modes as described in the following paragraphs. Fig. 6 shows the display for each of the three modes. It should be understood Fig. 6 represents either the A or B display. Both displays are capable of independent operation in any of the three modes.

3.31 Display interpretation is a key factor in using the instrument correctly. Careful study of Fig. 6 and the mode descriptions will aid greatly in understanding and using the instrument to maximum advantage.

3.32 Figure 6 is based on monitoring a DTMF (MF4) Touch Tone®) circuit as a typical example.

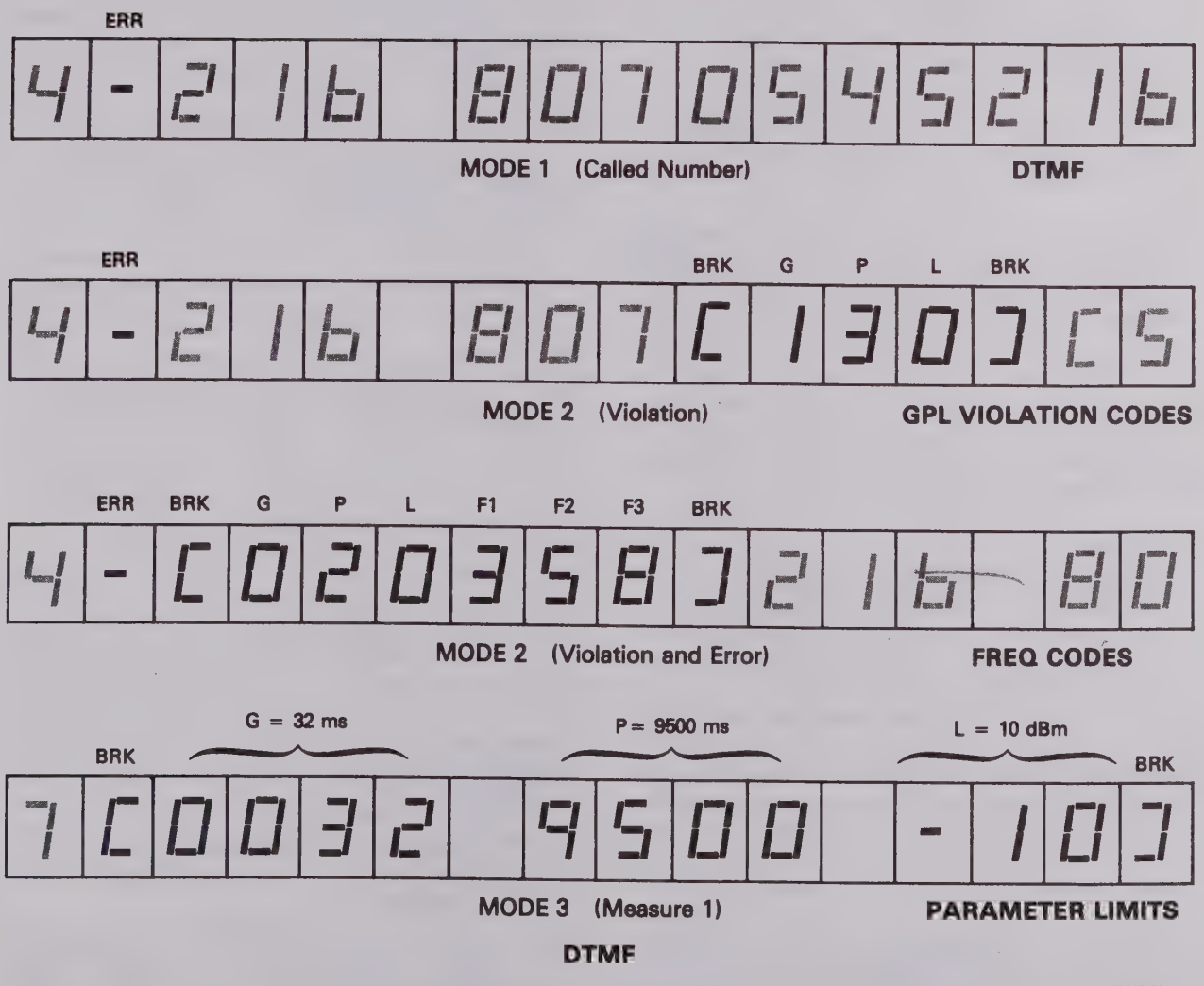


Fig. 6—Display Modes

3.33 Mode 1

3.34 MODE 1 (DIALED NUMBER): DISPLAY A and/or B shows the digits dialed by the calling party. A maximum of 16 digits may be shown on either display. Blanks are used to separate consecutive calls. A dash (-) represents an error. An error is a received digit with an incorrect number of tones. (See Fig. 6.)

3.35 Mode 2

3.36 MODE 2 (VIOLATIONS AND ERRORS): In this mode each digit received is checked for gap, pulse width, and level. These three parameters are known as the GPL data and are defined as follows:

G = Gap (Time between digits)
P = Pulse Width (Time duration of pulse)
L = Level (Transmission level)

Level applies only to AC (tone) signaling systems.

3.37 Violation

3.38 A GPL display will be generated for any digit which exceeds programmed upper and lower limits for gap, pulse width, or level. This is known as a violation.

3.39 The display will show three numerical violation codes enclosed in brackets (one for each parameter) following the digit with the violation. The violation codes are the same for all plug-in modules. (See Fig. 6.)

3.40 Error

3.41 In Mode 2 an error display will also be generated for any digit which does not contain the correct number of tones (error). This is in addition to the GPL violation codes. The display will show one or more (maximum eight) numerical frequency codes following the GPL violation codes. The GPL violation codes and frequency code(s) are enclosed by brackets. The frequency codes are different for the various plug-ins. (See Fig. 6.)

3.42 Mode 3

3.43 MODE 3 (MEASURE): In this mode the GPL parameters for each digit received are measured and the results displayed. The entire 16 character display is used for each digit. The display shows gap and pulse width in milliseconds and level in dBm. The gap, pulse width, and level readings are shown enclosed in brackets following the digit whose GPL values were measured. (See Fig. 6.)

3.44 When in Mode 2 or 3 the Model 2760 may be instructed to remove all brackets and the data between brackets from the display. The space vacated is then filled in by other received digits. This is known as a compressed display. This enables the viewing of up to 16 received digits. The display is now the same as in Mode 1. The brackets and data between brackets, removed from the display, are stored in memory and may be recalled later as desired.

3.45 Lead Digit Identification

3.46 LEAD DIGIT IDENT: Display is a three digit seven segment per digit LED display with a 0.125 inch character height. It is located midway between and just to the left of the A and B displays.

3.47 The Lead Digit Identifier (LDI) display will always show a number from 001 to 240. This number is a memory location or address. Depending upon the operation being performed the LDI identifies:

(a) DISPLAY A left hand (first) digit location in the register (address) signaling memory when monitoring traffic

(b) CURSOR location within the register (address signaling memory during recall of previously stored traffic

(c) Comparison memory location for the next digit when entering a series of digits for comparison with monitored traffic.

E. Indicators

3.48 There are two groups of LED indicators on the Model 2760 front panel. The two groups are located just to the left and right sides of the A and B DISPLAYS. The left hand group indicates the display status. The right hand group indicates the supervision conditions occurring as a monitored call progresses.

3.49 Display Status Indicators

3.50 Program Error

3.51 PRGM ERR: Flashes on and off to indicate a display assignment conflict exists. Each register (address) signaling plug-in module the mainframe assembly is equipped with must be assigned to

either the A or B DISPLAY. If two plug-in modules are assigned to the same display, an assignment conflict exists and the PRGM ERR indicator will flash on and off.

3.52 If two line (supervision) signaling plug-in modules are enabled the PRGM ERR indicator will again flash on and off because of the assignment conflict. The EN (enable) LED indicator on the register or line signaling plug-in modules may also flash on and off depending on which module it is.

3.53 Latch

3.54 LATCH: When lighted, indicates the instrument is in a hard latch state (hold). In this condition no additional register (address) signaling will be decoded. The A and/or B DISPLAYS are frozen until the hard latch state is cleared. The indicator remains on until a reset command is initiated.

3.55 Sequence Match

3.56 SEQ MAT: When lighted, indicates a digit sequence match has been detected. If any call sequence of digits on DISPLAY A matches a previously stored sequence of digits, the SEQ MAT indicator lights.

3.57 The comparison memory will hold up to 10 digit sequences. Each sequence may consist of up to 16 digits. The digits represent either a dialed number or supervision events.

3.58 The comparison memory is loaded with the desired digit sequences prior to traffic monitoring. When a match is detected the SEQ MAT indicator lights. If the HOLD MATCH switch was depressed the LATCH indicator will also light and DISPLAY A is frozen.

3.59 Signal Error

3.60 SIG ERR: When lighted, indicates an error or violation has been detected. If the HOLD ERROR switch was depressed the LATCH indicator will also light and the A and B DISPLAYS are frozen.

3.61 Supervision Indicators

3.62 There are six supervision indicators. The six indicators are:

SEIZURE
ANSWER
CLR FWD (Calling Party Connect)
CLR BACK (Called Party Hang-up)
RELEASE
BLOCKED (Busy).

These six LEDs indicate the supervision events occurring as a call progresses.

F. Latch States and Resets

3.63 A latch state is a hold condition. A latch state may be caused by:

(a) An operator action such as depressing the asterisk (*) key on the keypad or either of the CURSOR control pushbuttons.

(b) A plug-in module detecting a particular code or condition.

(c) Full register (address) signaling memories (NO ERASE switch is depressed).

3.64 In the latch state no additional register (address) signaling will be accepted, decoded, stored, or displayed. A reset command is necessary to clear the latch state. The LATCH indicator lights whenever the Model 2760 enters a latch state.

3.65 Soft Latch

3.66 A latch state is described as soft when it may be automatically cleared without operator intervention. A soft latch may be cleared by:

(a) A plug-in module detecting a particular code or condition.

(b) Depressing the RESET MAN pushbutton.

(c) A remote reset command.

The contents of the register (address) signaling memories are sent to a printer output port (Printer Control Module) whenever a soft latch occurs.

3.67 Hard Latch

3.68 A latch state is described as hard when operator intervention is required to clear it. A hard latch may be cleared by depressing the RESET MAN pushbutton or by a remote reset command.

G. Switches

3.69 The front panel of the Model 2760 is equipped with eight pushbutton switches located on the left hand side. The switches are of two types, momentary and push-push. They are used to perform the functions described in the following paragraphs.

3.70 Cursor

3.71 The CURSOR control consists of two momentary single action switches. Each switch has an arrow above it. One arrow points left (left hand switch) and the other arrow points right (right hand switch).

3.72 Momentarily depressing either switch activates the cursor and places the instrument into a hard latch (hold) state. The LATCH indicator will light. The cursor appears as a blinking vertical pair of digits on the A and B DISPLAYS. Only one digit blinks if only one display is in use.

3.73 Simultaneously the LEAD DIGIT IDENT (three digit display) will show the cursor position within the register (address) signaling memories. The plug-in register (address) signaling module(s) may also have lighted indicators for various parameters associated with the blinking digit(s).

3.74 Depressing either CURSOR switch moves the cursor left or right across the A and B DISPLAYS. The cursor moves at a speed of four characters per second (CPS) across the displays.

3.75 When the cursor reaches either end of the displays, two new groups of 16 digits each will appear on the displays. This process may be continued until the cursor reaches position 1 or position 240 in the register (address) signaling memories. Memory capacity is 24 digits. The cursor position in the memories is shown by the LEAD DIGIT IDENT display.

3.76 When both CURSOR switches are depressed the cursor jumps over blocks of 16 digits at a time. The cursor will jump four blocks per second. The LEAD DIGIT IDENT display will also jump in increments of 16 digits at a time, eg 001, 016, 032, etc. This enables rapid scanning of all 240 memory locations.

3.77 Both register (address) signaling memories are simultaneously scanned by the cursor. If the cursor is at position 64 in the A memory it is also at position 64 in the B memory. The A and B DISPLAYS may be thought of as 16 digit wide windows which may be moved back and forth across the A and B memories.

3.78 Recall Supervision

3.79 The RCL SUPV switch is a push-push double action switch. Depressing the switch places the contents of the supervision memory on DISPLAY A and the system clock time on DISPLAY B.

3.80 Supervision memory capacity is 16 digits. The digits are a code for supervision events. The code varies slightly for the different line (supervision) signaling plug-in modules. In general the supervision codes normally used are:

1 = Seizure
2 = Answer
3 = Clear Forward
4 = Clear Backward
5 = Release
6 = Blocked
0 = Idle.

3.81 Supervision events are stored in the supervision memory as a call progresses. They are also shown in real time on the six LED supervision indicators.

3.82 Supervision events may be displayed on the A DISPLAY in either Mode 1 or Mode 2. Some line (supervision) signaling plug-in modules do not provide Mode 2 displays. Compressed Mode 2 and Mode 3 displays are not provided for line (supervision) signaling plug-in modules.

3.83 During the time supervision events are being reviewed on DISPLAY A (system clock time on DISPLAY B) register (address) signaling will continue to be stored in memory. Releasing the RCL SUPV switch returns register (address) signaling digits to the A and/or B DISPLAYS.

3.84 Switching between register (address) and line (supervision) signaling displays may be done as often as desired. There is no loss of signaling information (digits/codes). Switching may be done as a call is in progress or after the call is completed.

3.85 A seizure condition marks the start of a call and an idle condition marks the end of a call. The supervision memory capacity is only 16 digits/codes. An idle condition or an overflow (more than 16 supervision events) locks out the supervision memory for the call.

3.86 The supervision memory is cleared by the next seizure condition if the RESET AUTO switch was depressed. Depressing the RESET MAN switch or a remote reset will also clear the memory.

3.87 The first digit/code stored in the supervision memory identifies the input port on which seizure was detected. There are a few exceptions to this, however, depending on the line (supervision) signaling plug-in module in use. The input ports are identified as follows:

1 = L1 (Line 1)
2 = L2 (Line 2)
3 = E Lead (SZ1-Sa-SR)
4 = M Lead (SZ2-Sb-SS)

3.88 Other designations for E&M leads are shown in parentheses. These are the known sets in use throughout the world.

3.89 System Clock Time

3.90 The Model 2760 is equipped with a built-in precision clock. When the instrument is first turned on, the clock begins counting elapsed time from power up. A 6 digit 24 hour format of hours, minutes, and seconds is used.

3.91 When the RCL SUPV switch is depressed, system clock time appears on the B DISPLAY. Initially, elapsed time from power up is shown. If desired, the internal clock may be set to the actual time of day. This is accomplished by entering the correct time of day via the keypad. The clock is accurate to ±1 second per hour.

3.92 No Erase

3.93 The NO ERASE switch is a push-push double action switch. When the NO ERASE and RESET AUTO switches are depressed the instrument will be in a soft latch state (hold) and upon completion (start of next call) will clear the supervision memory but not the register (address) signaling memories.

3.94 The second call's (called number) digits will be stored in memory, in sequence as received, next to the first call. The supervision memory will store supervision events for the second call.

3.95 If the NO ERASE switch is released a seizure condition will clear the supervision memory and the register (address) signaling memories also.

3.96 Hold Error

3.97 The HOLD ERROR switch is a push-push double action switch. When the HOLD ERROR switch is depressed any error in the received register (address) signaling will cause the instrument to enter a hard latch (hold) state. The latch occurs upon completion of the register (address) signaling.

3.98 Hold Match

3.99 The HOLD MATCH switch is a push-push double action switch. When the HOLD MATCH switch is depressed any digit sequence match detected will cause the instrument to enter a hard latch (hold) state. Comparison occurs after register (address) signaling is completed.

3.100 Both the HOLD ERROR and HOLD MATCH switches may be depressed when it is desired to catch errors and digit sequence matches. An error or digit sequence match will cause a hard latch.

3.101 Reset Automatic

3.102 The RESET AUTO switch is a push-push double action switch. When the RESET AUTO switch is depressed, individual plug-in modules will clear a soft latch (hold) state with an automatic reset. The trigger for this action is the receipt of the next supervision seizure condition.

3.103 Reset Manual

3.104 The RESET MAN switch is a momentary single action switch. When the RESET MAN switch is depressed all latch conditions (hard or soft) are cleared. The instrument is readied for the next call.

H. Keypad

3.105 The Model 2760 is equipped with a sixteen-button keypad. The keypad provides the means of performing the following functions:

(a) Setting the internal system clock time to the actual time of day

(b) Programming individual plug-in modules upper and lower limits for parameters such as gap, pulse width, and level (GPL), etc.

(c) Requesting a compressed display

(d) Programming the sequence comparison memory with up to 10 digit sequences to be compared with monitored calls

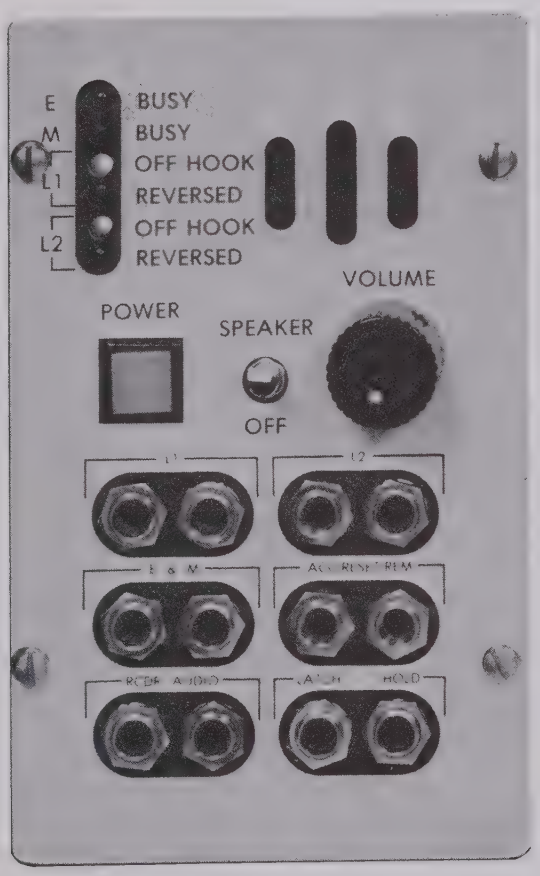
(e) Latch selection (one of nine possible latch conditions)

(f) Sequence match selection (one of eight possible sequence match conditions).

I. Resident Module

3.106 The Resident Module's front panel is shown in Fig. 7. The Resident Module is permanently installed in the Model 2760 mainframe assembly. It may be removed, however, for establishing initial reverse battery and E&M lead conditions by means of internal switch settings (See Part 2. INSTALLATION).

3.107 The Resident Module's primary function is to act as an interface unit between the circuits being tested and the plug-in modules. It also performs several other functions which are described in the following paragraphs.



968-02B

Fig. 7—Resident Module

3.108 Indicators

3.109 There are six LED indicators which provide Line 1 (L1), Line 2 (L2) and E&M lead status. The six indicators are:

(a) E OFF-HOOK (lighted for off-hook)

(b) M OFF-HOOK (lighted for off-hook)

(c) L1 OFF-HOOK (lighted for off-hook)

(d) L1 REVERSED (lighted for reverse battery)

(e) L2 OFF-HOOK (lighted for off-hook)

(f) L2 REVERSED (lighted for reverse battery).

3.110 Switches and Controls

3.111 The Resident Module is equipped with two switches and two controls as described in the following paragraphs.

(a) POWER: This switch is a red square double action push-push switch. It turns the instrument AC power on and off.

(b) SPEAKER OFF: Two position toggle switch which turns the speaker on and off. The speaker is mounted behind the three slots in the top of the front panel.

(c) VOLUME: This is a dual concentric potentiometer control. It controls the audible volume for Line 1 (L1) and Line 2 (L2) monitoring. The large knob is for L1 and the small center knob is for L2.

3.112 Jacks

3.113 The Resident Module is equipped with 12 type 310 jacks. The functions of these jacks are described in Table D.

TABLE D

RESIDENT MODULE JACKS

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
J1-J2	L1	Enable bridging connections to be made on the tip/ring leads of a circuit under test. Jacks are in parallel.
J3-J4	L2	Enable bridging connections to be made on the tip/ring leads of a circuit under test. Jacks are in parallel.
J5-J6	E&M	Enable bridging connections to be made on the E&M leads of a circuit under test (E lead on tips and M lead on rings). Jacks are in parallel.
J7	ACC-RESET	Applies contact closure (tip/ring short) to reset accessory equipment. Contact closure lasts for a duration of either the manual or the remote reset input.
J8	RESET-REM	Enables receiving a reset command from an external device. Reset command can be caused by shorting the tip/ring leads or by applying a resistive ground (less than 1 kohms) to the tip lead. Reset command must last 10 ms or more.
J9	RCDR	Outputs half-wave rectified signals suitable for strip chart recorder. Tip = L1 audio or forward audio if R2/MF2 receiver module is enabled. Ring = L2 audio or backward audio if R2/MF2 receiver module is enabled. Sleeve = chassis ground.
J10	AUDIO	Outputs combined L1 and L2 audio suitable for remote speaker or headset. Maximum output level is −10 dBm. Output level adjustable by VOLUME controls.
J11	LATCH	Outputs a contact closure (tip/ring short) for 256 ms to 512 ms when the Signaling Display enters a latch state.
J12	HOLD	Outputs a contact closure (tip/ring short) when: (1) an error has been detected if HOLD on ERROR switch is sent and/or (2) when a sequence match has been detected if HOLD on MATCH switch is set. Contact closure remains until removed by a reset command. May be used to activate an alarm bell or lamp when an error and/or sequence match is detected. Outputs a contact closure (tip/ring short) for 256 ms to 512 ms when an idle supervision condition has been detected if, and only if, both the HOLD on ERROR and HOLD on MATCH switches are released.

J. Plug-In Modules

3.114 There are currently 11 different plug-in modules available for the Model 2760 mainframe assembly. The available modules are:

2760-10 DP/SUPV RECEIVER (UNITED KINGDOM)
2760-11 DTMF REGISTER RECEIVER
2760-12 R2/MFC AND MF2 RECEIVER
2760-13 MF REGISTER RECEIVER
2760-14 CCITT NO. 5 REGISTER RECEIVER
2760-15 CCITT NO. 5 LINE RECEIVER
2760-16 CCITT NO. 4 REGISTER AND LINE RECEIVER
2760-17 SF RECEIVER (REGISTER AND LINE)
2760-18 AC9/AC11 RECEIVER (AC9 REGISTER AND LINE, AC11 LINE ONLY)
2760-20 DP/SUPV RECEIVER (NORTH AMERICAN)
2760-21 PRINTER CONTROL MODULE

3.115 The Model 2760 mainframe assembly is equipped with eight jacks for plug-in modules. It is very unlikely, however, that the mainframe would ever be equipped with eight plug-in modules.

3.116 A single width plug-in module is 1.5 inches (38 mm) wide. The various plug-in modules are single, double 3 inches (76 mm), triple 4.5 inches (114 mm) or quadruple 6 inches (152 mm) wide. Unequipped mainframe plug-in module jacks must be covered with blank dress panels (See Part 2. INSTALLATION).

3.117 Only two register (address) signaling modules and one line (supervision) signaling module may be enabled at the same time. There are only two register (address) signaling memories and one supervision memory provided.

3.118 The following paragraphs provide brief descriptions of the various plug-in modules. For detailed information consult the individual plug-in module manuals.

3.119 Model 2760-10-900 Dial Pulse and Supervision Receiver (UK)

3.120 ***Function.*** Receives one, or any two type(s) of dial pulse signaling from among the following selections: E-lead, M-lead, Loop on input line 1, Loop on input line 2. Handles both Loop and E&M supervision. Module is compatible with loop and E&M pulsing/supervision commonly used in the United Kingdom. (See 2760-20-900 module for North American version.)

3.121 Interface to Mainframe Displays

- Dial Pulsing: Mainframe displays digits 0 through 9; plus test digits 11 through 19 (shown as •1 through •9)

- Supervision Real-Time Display: Mainframe provides real-time LED display of Seizure, Answer, Clear Forward, Clear Back, Release, Blocked conditions

- Supervision Recall Display: Any of the above supervisory events plus Idle and Meter conditions can be stored by the mainframe for later review on the unit's row A. (Mainframe display includes number of Meter pulses received.) Unit stores up to 15 events per call.

3.122 Margin Test/Troubleshooting Features

3.123 The Model 2760-10-900 ignores pulses shorter than programmed minimum limit. Minimum acceptable pulse width is programmable from 20 to 99 milliseconds, in 1-millisecond increments.

3.124 Size

- Single-width plug-in (1.5 inches, 38 mm)

- Weight, approximately 1.3 pounds (0.6 kg)

3.125 Model 2760-11-900 DTMF Register Receiver

3.126 ***Function.*** Receives DTMF register signaling on 2-wire circuits. (This signaling system is commonly referred to as MF4 signaling in the United Kingdom and as Touch-Tone® or Digitone® signaling in North America.)

3.127 Interface to Mainframe Displays

3.128 Mainframe displays digits 0 through 9 plus codes A, B, C, D, #, and *. (Codes are displayed as •1 through •6.) Displays dash (-) for unrecognizable signals not composed of two, and only two tones.

3.129 Margin Test/Troubleshooting Features

3.130 Module can be programmed to include numerical error codes in the mainframe display of DTMF signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range. In addition, other error codes are provided to indicate received frequency components of any unrecognizable signals (not composed of two, and only two tones) displayed as a dash.

3.131 Programming also allows display of actual measured values of a, b, and c above for all DTMF signals received. All information is displayed in real time as detected, and is recallable from memory using mainframe's cursor controls.

3.132 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 697, 770, 852, 941, 1209, 1336, 1477, 1633 Hz
- Size: Triple-width plug-in (4.5 inches, 114 mm)
- Weight: Approximately 4.0 pounds (1.8 kg)

3.133 Model 2760-12-900 R2/MFC and MF2 Receiver

3.134 ***Function.*** Receives forward and backward register signaling on 2-wire and 4-wire R2/MFC or MF2 circuits. Receives forward register signaling on MF3 circuits.

3.135 Displays

3.136 LEDs show, for each forward and backward digit: (a) individual MF tones received, (b) any excessive delay (error) between forward and backward transitions, and (c) inrange/overrange tone level data. Information is displayed in real time as detected, and is recallable from memory using mainframe's cursor controls.

3.137 Interface to Mainframe Displays

3.138 Mainframe displays digits/codes 0 through 15 (11 through 15 displayed as 1 through 5); displays uppercase dash (¯) for MF2/MF3 forward prefix 14 and lowercase dash (_) for MF2 backward prefix 9. Signals violating a programmed maximum acceptable receive level (overrange), or violating a programmed minimum acceptable tone duration, are displayed as a blank space while signals not consisting of two, and only two tones are displayed as a dash (-).

3.139 Margin Test Troubleshooting Features

- Delay: recognizes as a signaling error any forward/backward or backward/forward delay exceeding setting of delay control; adjustable from 1 to 19 seconds.
- Minimum Tone Duration: ignores any signal shorter than 20 milliseconds; displays blank space for any digit, code, or signal shorter than setting of minimum tone duration control but longer than 20 milliseconds; minimum control adjustable from 20 to 99 milliseconds.
- Forward/Backward Receive Thresholds: independent threshold controls for forward and backward signals; each adjustable from 0 to −35 dBm (ref. 600 ohms). Any signal 0.5 dB lower or 12.5 dB higher than the threshold setting is out of range and is not displayed. Underrange signals are ignored and overrange signals are displayed as a blank.

3.140 Sensitivity

- Manual Mode: recognition sensitivity depends on settings of forward and backward threshold controls; range of 0 to −35 dBm (ref. 600 ohms)
- AGC Mode: recognizes signals over dynamic range between upper threshold of +3 dBm and selectable lower threshold of −26 or −35 dBm.

3.141 Frequency Detection

- Receives all 12 R2/MFC, MF2, and MF3 frequencies ±20 Hz
- Size: Four standard module widths (6 inches, 152 mm)
- Weight: Approximately 5 pounds (2.3 kg)

3.142 Model 2760-13-900 R1 MF Register Signaling Receiver

3.143 ***Function.*** Receives R1 (standard North American MF) register signaling digits and codes on 2-wire or 4-wire circuits.

3.144 Interface to Mainframe Displays

3.145 Mainframe displays digits 0 through 9, ST3P, STP, KP, ST2P, and ST (codes are displayed as •1 through •5). Displays dash (-) for unrecognizable signals not composed of two, and only two tones.

3.146 Margin Test/Troubleshooting Features

3.147 Module can be programmed to include numerical error codes in the mainframe display of register signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range. In addition, other error codes are provided to indicate received frequency components of any unrecognizable signals (not composed of two, and only two tones) displayed as a dash.

3.148 Programming also allows display of actual measured values of a, b, and c above for all register signals received. All information is displayed in real time as detected, and is recallable from memory using the mainframe's cursor controls.

3.149 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 700, 900, 1100, 1300, 1500, 1700 Hz ± 20 Hz
- Size: Double width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.150 Model 2760-14-900 CCITT #5 Register Signaling Receiver

3.151 ***Function.*** Receives CCITT #5 register signaling digits and codes on 2-wire or 4-wire circuits.

3.152 Interface to Mainframe Displays

3.153 Mainframe displays digits 0 through 9, Code 11, Code 12, KP1, KP2, and ST (codes are displayed as •1 through •5). Displays dash (-) for unrecognizable signals not composed of two, and only two tones.

3.154 Margin Test/Troubleshooting Features

3.155 Module can be programmed to include numerical error codes in the mainframe display of register signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range. In addition, other error codes are provided to indicate received frequency components of any unrecognizable signals (not composed of two, and only two tones) displayed as a dash.

3.156 Programming also allowed display of actual measured values of a, b, and c above for all register signals received. All information is displayed in real time as detected, and is recallable from memory using the mainframe's cursor controls.

3.157 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 700, 900, 1100, 1300, 1500, 1700 Hz ± 20 Hz
- Size: Double-width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.158 Model 2760-15-900 CCITT #5 Supervision Receiver

3.159 ***Function.*** Receives CCITT #5 supervision/control signals (2400 and 2600 Hz) on 4-wire circuits.

3.160 Interface to Mainframe Displays

- Real-Time Display: Mainframe provides real-time LED display of Seizure, Double Seizure, Answer, Clear Forward, Clear Back, Release, Blocked (Busy) conditions.
- Recall Display: Any of the above supervisory events plus Idle, Acknowledge, Forward Transfer, and Proceed to Send conditions can be stored by the mainframe for later review on the analyzer's row A. Analyzer stores up to 15 events per call.

3.161 Margin Test/Troubleshooting Features

3.162 Module can be programmed to include numerical error codes in the mainframe recall display of supervisory signals violating specified limits for pulse width and received level. Limits are programmable over a wide range.

3.163 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 2400 and 2600 Hz ± 20 Hz
- Size: Double-width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.164 Model 2760-16-900 CCITT #4 Register and Supervision Receiver

3.165 ***Function.*** Receives CCITT #4 register signaling and/or supervision/ control signals (2040 and 2400 Hz) on 4-wire circuits.

3.166 Interface to Mainframe Displays

- Register Signaling: Mainframe displays digits/codes 0 through 15 (11 through 15 and 0 displayed as 1 through 6); displays dash (-) for register signals not composed of four, and only four elements (bits). Also provides display of Acknowledgement and Number Received signals sent in backward direction. (Number Received is normally defined as a supervisory signal, but for convenience is displayed as part of the register signaling sequence).
- Supervision Real-Time Display: Mainframe provides real-time LED display of Terminal and Transit Seizure, Answer, Clear Forward, Clear Back, Release, Blocked (Busy) conditions.
- Supervision Recall Display: Any of the above supervisory events plus Idle, Terminal and Transit Proceed to Send, and Forward Transfer conditions can be stored by the mainframe for later review on the analyzer's row A. Invalid supervisory signals are displayed as a dash (-).

3.167 Margin Test/Troubleshooting Features

3.168 Module can be programmed to include numerical error codes in the mainframe display of CCITT #4 signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range. In addition, other error codes are provided to indicate elements or frequencies received for invalid register or supervisory signals displayed as a dash.

3.169 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 2040 and 2400 Hz ± 20 Hz
- Size: Double-width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.170 Model 2760-17-900 SF Register and Supervision Receiver

3.171 ***Function.*** Receives North American 2600 Hz SF pulsing and/or supervisory signals on 4-wire circuits. Module is compatible with CCITT R1 line signaling.

3.172 Interface to Mainframe Displays

- Register Signaling: Mainframe displays digits 0 through 9
- Supervision Real-Time Display: Mainframe provides real-time LED display of Seizure, Glare, Answer, Calling Party Disconnect (Clear Forward), Called Party Hang-up (Clear Back), and Busy (Blocked) conditions
- Supervision Recall Display: Any of the above supervisory events plus Idle, and Wink (and similar signals such as Delay-Dial or Start-Dial) conditions can be stored by the mainframe for later review on the analyzer's row A. Analyzer stores up to 15 events per call.

3.173 Margin Test/Troubleshooting Features

3.174 Module can be programmed to include numerical error codes in the mainframe display of SF register and supervisory signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range.

3.175 All information is displayed in real time as detected, and is recallable from memory using mainframe's cursor controls.

3.176 Reception Parameters

- Dynamic Range: −40 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 2600 ± 20 Hz
- Size: Double width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.177 Model 2760-18-900 AC9/AC11 Supervision and Pulsing Receiver

3.178 ***Function.*** Receives AC11 supervision/control signals and AC9 signaling (2280-Hz pulsing with 4-wire 2280 Hz supervision). Accepts both-way working circuits.

3.179 Interface to Mainframe Displays

- Register Signaling (AC9): Mainframe displays digits 0 through 9
- Supervision Real-Time Display (AC9/AC11): Mainframe provides real-time LED display of Seizure, Answer, Clear Forward, Clear Back, Release, Blocked conditions
- Supervision Recall Display (AC9/AC11): Any of the above supervisory events plus Idle, Seize 2, and Check Tone conditions can be stored by the mainframe for later review on the analyzer's row A. Analyzer stores up to 15 events per call.

3.180 Margin Test/Troubleshooting Features

3.181 Module can be programmed to include numerical error codes in the mainframe display of AC9/AC11 signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. Limits are programmable over a wide range.

3.182 All information is displayed in real time as detected, and is recallable from memory using mainframe's cursor controls.

3.183 Reception Parameters

- Dynamic Range: −26 to +6 dBm (ref. 600 ohms)
- Frequency Detection: 2280 ± 25 Hz
- Size: Double-width plug-in (3 inches, 76 mm)
- Weight: Approximately 3.0 pounds (1.4 kg)

3.184 Model 2760-20-900 Dial Pulse and Supervision Receiver (North American)

3.185 ***Function.*** Receives one, or any two types of dial pulse signaling from among the following selections: E-lead, M-lead, Loop on input line 1, Loop on input line 2. Handles both Loop and E&M supervision. Module is compatible with Loop and E&M pulsing/supervision commonly used in North America. (See 2760-10-900 module for United Kingdom version.)

3.186 Interface to Mainframe Displays

- Dial Pulsing: Mainframe displays digits 0 through 9. (Actually, digits up to 19 can be displayed if, for any reason, they appear on a line being monitored.
- Supervision Real-Time Display: Mainframe provides real-time LED display of Seizure, Wink (and similar signals such as Delay-Dial or Start-Dial), Answer, Calling Party Disconnect (Clear Forward), and Called Party Hang-Up (Clear Back) conditions.
- Supervision Recall Display: Any of the above supervisory events plus Idle condition can be stored by the mainframe for later review on the unit's row A. Unit stores up to 15 events per call.

3.187 Margin Test/Troubleshooting Features

- Ignores pulses shorter than programmed minimum limit. Minimum acceptable pulse width is programmable from 20 to 99 milliseconds, in 1-millisecond increments.
- Size: Single-width plug-in (1.5 inches, 38 mm)
- Weight: Approximately 1.3 pounds (0.6 kg)

3.188 Model 2760-21-900 Printer Control

3.189 ***Function.*** This module enables hard-copy printout of all signaling/supervision events monitored by the analyzer. It provides an ASCII coded output compatible with a wide variety of teleprinters or other input/output devices. Northeast Electronics makes available Texas Instruments Model 743 teleprinter control module). Numerous data storage and analysis features are built into the module for service observation, troubleshooting, and many other applications.

3.190 Detailed call progress data can be printed for all calls monitored or for only those calls meeting certain specified report criteria . . . error status, direction of seizure, time/date, others. Thus, reports are prescreened listing only calls of interest. Besides the actual signaling/supervision events monitored, each call report contains other pertinent information such as date and time of call, job, name/number, error codes, and measured values for key signaling and timing parameters. User programming allows selection of print criteria and report format to exactly suit the needs of individual applications.

3.191 The printer control plug-in also stores peg count data for all calls monitored. Stored total counts can be printed at any time upon demand. This information is valuable whenever call completion statistics are desired.

3.192 In addition to a teleprinter interface, the printer control module provides other inputs/outputs for use with downstream processing devices, multiline concentrators, and similar equipment that may be needed in certain applications.

3.193 Selectable Print Criteria

- ***Seizure.*** Prints only those calls where seizure occurs on the specified 2760 input port: Line 1, Line 2, E-lead, or M-lead.
- ***Event.*** Prints only those calls where the specified event occurred: sequence match, sequence mismatch, signaling error, no signaling error, selected supervisory event present, or selected supervisory event absent.
- ***Time.*** Prints only those calls occurring: (1) during specified day, (2) anytime except specified day, (3) during specified hours, or (4) outside specified hours. If alternative (3) or (4) is selected, user may further specify (a) printing of all calls monitored during time of interest and no calls during other times, or (b) printing all calls monitored during time of interest and only those calls meeting event criterion during other times, or (c) printing only calls meeting event criterion during time of interest and no calls during other times.

3.194 Selectable Report Formats

- Format 1. Prints for each monitored call: date, job name and number, all signaling and supervision events, time of seizure, call holding time (answer to idle), total seizure time
- Format 2. Prints for each monitored call: date, job name and number, all signaling and supervision events, error codes for violation of acceptable limits for no-tone gap, pulse width, received level (if any)
- Format 3. Prints for each monitored call: date, job name and number, all signaling and supervision events, measured values for no-tone gap, pulse width, received level.

3.195 Summary Report Printout

3.196 Gives peg count data for up to 9,999 calls. Report contains the following information: (1) time of report, (2) total seizures observed, (3) total completed calls, (4) total calls meeting print criteria and therefore resulting in hard-copy printout, (5) total calls violating preprogrammed limits for normal call timing. User can specify acceptance thresholds for the following normal call timing parameters: (a) maximum wait for answer time, (b) maximum completed call holding time, (c) minimum completed call holding time.

3.197 Other Features

3.198 Other features include programmable 2760 reset conditions, inputs/outputs for downstream processing devices and multiline concentrators.

3.199 Teleprinter Interface

- Type: Serial ASCII, EIA RS232-C or 20-milliampere current loop. Programmable baud rate, parity condition, number of data bits.
- EIA Configuration: Data Terminal Equipment (DTE). A 4-foot (1.22-m) null modem cable supplied with plug-in provides a Data Communication Equipment (DCE) interface.
- Stop Bits: Module sends two stop bits; receives one or more.
- Size: Single-width plug-in (1.5 inches, 38 mm)
- Weight: Approximately 1.3 pounds (0.6 kg)

K. Rear Panel

3.200 Fig. 8 shows the Model 2760 rear panel layout. Items mounted on the rear panel are described in Table E.

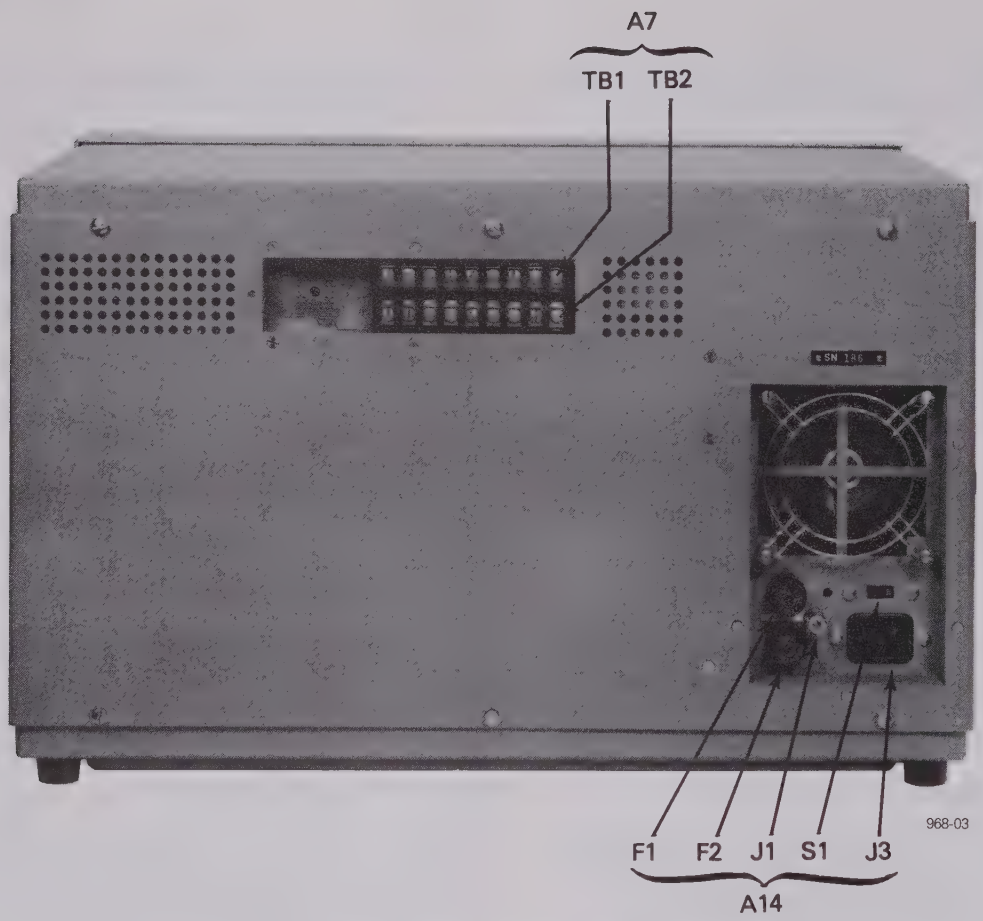


Fig. 8—Rear Panel Controls and Connectors

TABLE E

REAR PANEL ITEMS

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
TB1/TB2	barrier strip terminals	Provides screw contacts for hard wiring input/output connections in permanent installation. Connected in parallel with front panel input/output jacks.
F1/F2	1A or 2A 250 V slow-blow fuses	Protect against excessive input current. Use 2A fuses for 115 Vac operation. Use 1A fuses for 230 Vac operation.
J1	ground jack	Provides method of connecting test set to CO ground.
J3	3-pin ac power connector	Connects 2760 to an ac power source.
S1	115/230 slide switch	Configures the 2760 for 115 or 230 Vac operation.

L. Specifications

3.201 Table F gives the Model 2760 mainframe assembly specifications.

TABLE F

SPECIFICATIONS

DISPLAY A	16 character alphanumeric display
Type	7 segment plus dp (LED)
Refresh Rate	62.5 Hz
DISPLAY B	16 character alphanumeric display
Type	7 segment plus dp (LED)
Refresh Rate	62.5 Hz
LEAD DIGIT IDENT	3 digit display 001-240
Type	7 segment plus dp (LED)
Refresh Rate	62.5 Hz
Real Time	Identifies DISPLAY A left hand digit location in register (address) signaling memory
Recall	Identifies CURSOR location in register (address) signaling memory
Sequence Comparison	Identifies next digit in sequence to be entered
REGISTER (ADDRESS) SIGNALING	
Real Time	DISPLAY A and/or DISPLAY B shows up to 16 of the most recent digits/codes received
Recall	Up to 240 digits/codes received may be recalled from register (address) signaling memory and shown (16 at a time) on DISPLAY A and/or DISPLAY B.
Memory Capacity (A)	240 digits/codes DISPLAY A
Memory Capacity (B)	240 digits/codes DISPLAY B
CURSOR ← →	2 momentary pushbutton switches used to recall register (address) signaling digits/codes from memory. CURSOR appears as a blinking (2 Hz) vertical pair of digits/codes on DISPLAY A and DISPLAY B. Information appearing on plug-in modules pertains to the blinking pair of digits/codes. LEAD DIGIT IDENT display indicates CURSOR CURSOR location in memory.
← Depressed	CURSOR moves to left at 4 CPS.
→ Depressed	CURSOR moves to right at 4 CPS.
← → Both depressed	CURSOR moves in increments of 16 digits/codes at a time (4 Hz) towards memory location 1 or 240.
	DISPLAY A and DISPLAY B are in effect 16 digits/codes wide windows which move together across the register (address) signaling memory locations (1-240)

TABLE F (Cont)

SEQUENCE COMPARISON	Up to 10 sequences (addresses of called numbers) may be entered via the keypad and stored in memory. Each sequence may have up to 16 digits/codes. Any match in monitored traffic causes the Model 2760 to halt operation and/or initiate an alarm.
LINE (SUPERVISION) SIGNALING	
SEIZURE ANSWER CLR FWD (Calling party disconnect) CLR BACK (called party hang-up) RELEASE BLOCKED (Busy)	6 LEDs indicate in real time the designated supervision event as the call progresses
RCL. SUPV.	Push-push switch
Released Store	Up to 16 supervision digits/codes are stored in line (supervision) signaling memory as call progresses.
Depressed Recall	DISPLAY A shows up to 16 supervision digits/codes as recalled from line (supervision) signaling memory. DISPLAY A left hand digit (1 – 4) identifies mainframe input port on which signal occurred: 1 = Line 1 2 = Line 2 3 = E lead 4 = M lead
System Time	DISPLAY B shows hours, minutes and seconds, 24 hour format, accuracy ±1 second/hour.
Real Time	If RCL SUPV switch is depressed before call begins, DISPLAY A shows supervision digits/codes in real time as received. The digits/codes are also stored in line (supervision) signaling memory.
Memory Capacity	16 digits/codes
DISPLAY STATUS	4 LEDs indicate the status of the A and B displays.
PRGM ERR	Blinks to indicate plug-in modules are incorrectly enabled.
LATCH	Indicates latch state exists. No register (address) signaling accepted until latch is cleared.
SEQ MAT	Indicates a sequence comparison match has occurred.
SIG ERR	Indicates a signaling error has been detected.

TABLE F (Cont)

CIRCUIT STATUS	6 LEDs indicate the status of the circuit being tested. When lighted:
E OFF HOOK	Indicates E lead seizure
M OFF HOOK	Indicates M lead seizure
L1 OFF HOOK	Indicates Line 1 is off-hook
L1 REVERSED	Indicates Line 1 reverse battery
L2 OFF HOOK	Indicates Line 2 is off-hook
L2 REVERSED	Indicates Line 2 reverse battery
INPUT IMPEDANCE	
L1 and L2	50 Kohms (500 Vdc max)
E and M	200 Kohms each
INPUT/OUTPUT CONTROL SIGNALS	
REM RESET (Input)	Tip-ring closure or resistive ground on tip (less than 1 kohm) for at least 10 milliseconds. Resets Signaling Display remotely.
ACC RESET (Output)	Tip-ring closure for duration of REM RESET input or for duration of MAN RESET.
Contact Rating	0.5 Amp at 250 Vac maximum.
RCDR (Output)	Half wave rectified signal suitable for driving strip chart recorder. Line L1 signaling on tip and line L2 signaling on ring. Chassis ground on sleeve.
Output Impedance	Approximately 1 kohm.
AUDIO (Output)	Combined line L1 and line L2 signaling.
Output Level	+7.5 dBm maximum, level of each line adjustable with separate volume controls.
LATCH (Output)	Tip-ring closure for 256-512 milliseconds when Signaling Display enters a latch state.
Contact Rating	0.5 Amp at 250 Vac maximum.
HOLD (Output)	Tip-ring closure until reset when: 1. Signal error is detected and HOLD ERROR switch is depressed. 2. Sequence match is detected and HOLD MATCH switch is depressed. Tip-ring closure for 256-512 milliseconds if input circuit becomes idle and neither HOLD switch is depressed.
Contact Rating	0.5 Amp at 250 Vrms maximum.

TABLE F (Cont)

INPUT/OUTPUT CONNECTIONS	
Line L1 or L2	Two front panel jacks and rear panel terminal punchings connected in parallel (tip-to-tip and ring-to-ring). Jacks accept type 310 plugs.
E&M	Two front panel jacks and rear panel terminal punchings connected in parallel (E lead on tip, M lead on ring). Jacks accept type 310 plugs.
REM RESET (Input) ACC RESET (Output) RCDR (Output) AUDIO (Output) LATCH (Output) HOLD (Output)	Each front panel jack connected in parallel with rear panel terminal punchings. Jacks accept type 310 plugs.
PHYSICAL CHARACTERISTICS	
Size	26.7 cm h x 43.2 cm w x 30.5 cm d (10.5 in h x 17 in w x 12 in d)
Weight	Approximately 11.3 kg (25 lbs)
PLUG-IN MODULES	
CAPACITY	Up to 8 single-width modules; single-width = 3.8 cm (1.5 in)
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature	5°C to 40°C (41°F to 104°F)
Relative Humidity	0 to 95% non-condensing
POWER REQUIREMENTS	
AC Power	115 ± 10 Vac, 47 to 63 Hz or 230 ± 20 Vac, 47 to 63 Hz switch selectable. 100 Watts
Fuse	S10 Blow 2A 115 Vac S10 Blow 1A 230 Vac
AC Input	115/230 Vac recessed jack J3 located on rear panel.

4. OPERATION

A. General

4.01 This part describes how to use and operate the Model 2760 Universal Signaling Analyzer. Figure 9 is an overall functional block diagram of the instrument.

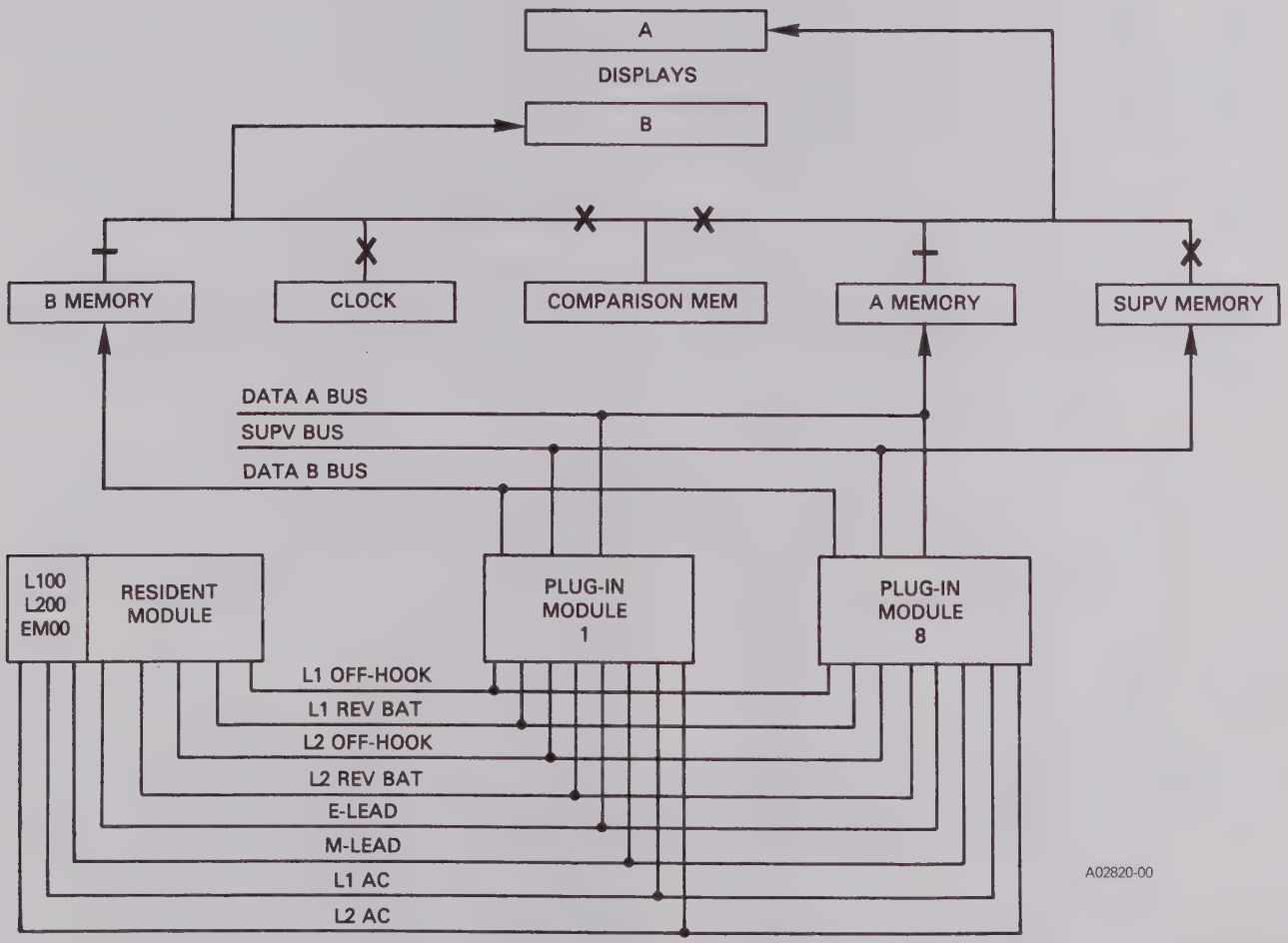


Fig. 9—Functional Block Diagram

B. Internal Switch Settings

4.02 The Resident Module contains internal switches which determine the conditions for reverse battery and E&M lead on-hook and off-hook supervision. The switch settings MUST match the conditions encountered on the circuits to be tested. See Part 2. INSTALLATION for the switch setting procedures.

C. Plug-In Module Selection

4.03 The Model 2760 mainframe assembly must be equipped with the appropriate plug-in modules for the circuits to be tested. Since the mainframe can operate with two register (address) signaling modules and one line (supervision) signaling module enabled, it may be used on circuits having many different combinations of signaling.

4.04 As an aid in selecting the appropriate plug-in modules, Table G lists some of the possible signaling combinations which may be encountered. The first two columns show register signaling and the third column shows possible types of line signaling for that combination of register signaling.

4.05 Some plug-in modules are capable of monitoring register signaling as well as line signaling. These plug-in modules may be instructed to perform the two monitoring functions together or separately.

4.06 Table H lists the plug-in module characteristics. Part 3. DESCRIPTION provides a brief description of the 11 available plug-in modules.

4.07 From the information given in Tables G and H select the required plug-in modules for the circuits to be tested. Carefully insert the selected modules into the mainframe assembly. Make sure each module is fully seated in its respective jack.

4.08 The modules may be inserted into the mainframe in any order as all plug-in module jacks are wired in parallel. Make sure all of the plug-in module ENABLE switches are released (not depressed).

Warning: Any unused plug-in module jacks must be covered by dress panels to insure proper air flow through the instrument. Failure to heed this warning may result in damage to the equipment.

TABLE G

REGISTER SIGNALING AND LINE SIGNALING COMBINATIONS

A DISPLAY	B DISPLAY	SUPERVISION	REMARKS
R2F	R2B	EM, AC11	
R2F	L2	EM, AC11, LP	
R2F	E or M	EM, AC11	
R2F	AC9	EM, AC11	Refer to note 1,6
R2F	#4	EM, AC11, #4	Refer to note 1
R2F	MF	EM, #5	Refer to note 1
R2F	TT	EM, AC11, LP	Refer to note 2
L1	L2	LP	Refer to note 3
L1	E or M	LP, EM	
L1	AC9	LP, EM, AC9	Refer to note 4,6
L1	#4	LP, EM, #4	Refer to note 4
L1	MF	LP, EM, #5	Refer to note 4
L1	TT	LP	
L1	MF3	LP, EM, AC11	
E	M	EM	
E or M	AC9	EM, AC11	
E or M	#4	EM, #4	
E or M	MF	EM, #5	
E or M	TT	EM, LP	
E or M	MF3	EM, AC11	

TABLE G (Cont)

A DISPLAY	B DISPLAY	SUPERVISION	REMARKS
AC9	#4	EM, AC11, #4	Refer to note 4,6
AC9	MF	EM, AC11, #5	Refer to note 4,6
AC9	TT	EM, AC11, LP	Refer to note 2,6
AC9	MF3	EM, AC11	
#4		#4, EM	
#4	MF	#4, EM, #5	Refer to note 4
#4	TT	#4, EM, LP	Refer to note 2
#4	MF3	#4, EM, AC11	Refer to note 4
MF		#5, EM, LP	Refer to note 6
MF	TT	#5, EM, LP	Refer to note 2
MF	MF3	#5, EM, AC11	Refer to note 5
TT	MF3	LP, EM, AC11	

ABBREVIATIONS USED IN TABLE

Types of register signaling (address)

R2F	R2/MFC or MF2 forward	AC9	2280-Hz pulsing (Refer to note 6)
L1	Loop dial pulsing on Line L1	MF	CCITT #4 pulsing
L2	Loop dial pulsing on Line L2	MF	CCITT #5 pulsing or R1
E	Dial pulsing on E lead	TT	Touch Tone® (MF4, DTMF)
M	Dial pulsing on M lead	MF3	MF3

Types of line signaling (supervision)

EM	E&M
LP	loop
AC11	AC11 (2280– Hz)
#4	CCITT #4 (2040-Hz, 2400-Hz)
#5	CCITT #5 (2400-Hz, 2600-Hz)

Notes:

1. Some R2/MFC or MF2 signaling systems require two input line ports (4-wire). One input line (normally the backward signaling, R2B) may be sacrificed to allow other types of signaling systems to have access to the B display. Thus all combinations of register signals can be displayed.
2. Touch Tone® normally uses loop supervision.
3. Supervision at input port L2 is not displayed.
4. AC11, #4, #5 are four-wire line signaling (supervision) types requiring two input ports (L1, L2) for full two-way supervision monitoring and display. LP line signaling requires only one input port (L1 or L2), and EM line signaling is applied at a separate input port (E&M). When monitoring a four-wire signaling type together with another type (either four-wire or two-wire) it is necessary to either short together the two four-wire systems or to connect only one two-wire input line from each system to the Signaling Display. This means that part of the signaling (on each neglected pair) is unavailable for monitoring storage. Except for incomplete supervision analysis, the Signaling Display can monitor and display register signaling for all combinations listed in the table.
5. Loop supervision is used on AT&T Long Lines system and also on CAMA ANI/ONI trunks.
6. AC9 implies both pulsing and supervision are composed of 2280 Hz tone bursts.

TABLE H

PLUG-IN MODULES

MODEL	DESCRIPTION
2760-10-900	Dial Pulse and Supervision Receiver (UK)
2760-11-900	DTMF Register Receiver (MF4 Touch Tone®)
2760-12-900	R2/MFC and MF2 Receiver
2760-13-900	R1 MF Register Signaling Receiver
2760-14-900	CCITT #5 Register Signaling Receiver
2760-15-900	CCITT #5 Supervision Receiver
2760-16-900	CCITT #4 Register and Supervision Receiver
2760-17-900	SF Register and Supervision Receiver
2760-18-900	AC9/AC11 Supervision and Pulsing Receiver
2760-20-900	Dial Pulse and Supervision Receiver (North America)
2760-21-900	Printer Control

Note:

1. There is no 2760-19-900 module.

D. Verification Tests

4.09 Verification tests enable the operator to verify that the instrument is in good working order prior to any circuit testing.

4.10 Initial Conditions

4.11 Make sure all of the following conditions are met before proceeding with the verification tests.

(a) Instrument is correctly fused and rear panel switch is set for the appropriate voltage (115/230).

Warning: The instrument may be severely damaged if the fuse or switch setting is incorrect.

(b) Instrument is plugged in to an AC electrical power source of the correct voltage (3-wire grounded type outlet).

(c) Ground binding post on rear panel is connected to central office ground bus. No. 14-AWG wire is recommended.

(d) The following front panel pushbutton switches are released:

RCL SUPV
NO ERASE
HOLD ERROR
HOLD MATCH
RESET AUTO

(e) All plug-in module ENABLE switches are released.

(f) Instrument is not connected to any circuits to be tested.

4.12 Power Up

4.13 This test verifies AC power has been correctly applied to the instrument:

STEP	PROCEDURE
1	Depress POWER switch.
	Verification:
	Blower fan runs LEAD DIGIT IDENT shows 001 L1 OFF HOOK lights L2 OFF HOOK lights.

4.14 Cursor

4.15 This test verifies the cursor is operating properly:

STEP	PROCEDURE
1	Depress and hold right hand CURSOR switch. Verification: LATCH indicator lights. LEAD DIGIT IDENT counts to 240 (requires approximately one minute).
2	Release switch.
3	Depress and hold left hand CURSOR switch. Verification: LEAD DIGIT IDENT counts backward from 240 to 001 (requires approximately one minute).
4	Depress and release RESET MAN switch. Verification: LATCH indicator is extinguished.

4.16 System Clock

4.17 This test verifies the internal system clock is operating properly:

STEP	PROCEDURE
1	Depress the RCL SUPV switch. Verification: System clock time shown on B DISPLAY six digit 24 hour format of hours, minutes, and seconds. Time shown is elapsed time since power up.
2	Release RCL SUPV switch. Verification: B DISPLAY goes blank.

4.18 A and B Displays and Keypad

4.19 This test verifies that the DISPLAYS and KEYPAD are functioning properly:

STEP	PROCEDURE
1	Depress KEYPAD asterisk (*) key. Verification: LATCH indicator lights.
2	Depress KEYPAD (A) key and then (0) key.
3	Depress KEYPAD keys (1), (2), (3), (4), (5), (6), (7), (8), (9), and (0) in order. Verification: Digits appear in order on A DISPLAY. LEAD DIGIT IDENT counts to 011.
4	Depress KEYPAD keys (1), (2), (3), (4), (5), and (6) in order. Verification: Digits appear in order entered on A DISPLAY. Digits are duplicated on B DISPLAY. Last digit 6 blinks (cursor) on both displays. LEAD DIGIT IDENT counts to 016 and drops to 001 when key (6) is depressed.
5	Depress (c) key. Verification A DISPLAY goes blank.
6.	Depress pound (#) key. Verification: B DISPLAY goes blank.
7	Depress RESET MAN switch. Verification: LATCH indicator extinguished.

4.20 To check the seven segments of all 32 LED alphanumeric character readout devices, repeat the above procedure using only the digit (8) key in step 3. Depress the (8) key 16 times. Skip step 4.

4.21 To check digits •1 to •9 repeat the procedure in paragraph 4.19 and key an (*) ahead of each digit. For example, keying (*1) will appear as •1 on the display. (*0) is an impossible condition.

4.22 Comparison Memory

4.23 This test checks the digit comparison memory for proper operation. The memory is made up of 10 files. Each file will hold 16 digits. The files are numbered A0 to A9.

4.24 To check each of the 10 files, repeat the procedure in paragraph 4.19 ten times. Change the file number in step 3 each time beginning with A0, then A1, A2, etc. until all 10 files have been checked. If the 16 digits on the A DISPLAY are duplicated on the B DISPLAY the file is functioning properly.

4.25 Plug-In Modules

4.26 This test verifies the operating condition of each plug-in module. For each module in turn:

STEP	PROCEDURE
1	Depress the ENABLE pushbutton switch. Verification: EN indicator lights.
2	Depress the PROGRAM pushbutton switch. Verification: Various readouts will appear on the A and/or B DISPLAYS. These readouts are the initial conditions for display modes and latches and initial parameter limits programmed into each plug-in module.
3	Release the ENABLE pushbutton switch. Verification: Display goes blank.
4	Repeat steps 1 through 3 for each plug-in module.

E. General Operating Procedures

4.27 Always make sure the front panel switches are conditioned as shown below prior to beginning each of the programming procedures:

RCL SUPV	Released
NO ERASE	Released
HOLD ERROR	Released
HOLD MATCH	Released
RESET AUTO	Released

4.28 Also make sure no plug-in modules are enabled. All plug-in module ENABLE switches must be released. Failure to follow these precautions will cause incorrect responses. Finally, always depress the RESET MAN switch to clear any hard latch state which may exist.

F. Keypad Programming

4.29 The operation of the Model 2760 is controlled by front panel switches and instructions and data keyed into the instrument by means of the KEYPAD. The instructions and data may be separated into three groups as follows:

GROUP 1: Setting the internal system clock to the correct time of day.

GROUP 2: Specifies the signaling (either register or line) digit sequences to be stored in the comparison memory files.

GROUP 3: This group is subdivided as follows:

1. Selecting which latch request from a plug-in module to acknowledge. When the acknowledgement is made a soft latch state occurs.

2. Selecting the type of digit sequence comparison (match) to be made once the soft latch state exists.

3. DISPLAY B Memory Reformat Programming.

4. Changing a Mode 2 or 3 display into a compressed display.

4.30 Briefly, KEYPAD programming begins when the "*" key is pressed. At that time, the 2760 enters into a hard latch state and the LATCH indicator lights. To exit keypad programming, the "#" key is pressed (in one instance the "#" key must be pressed twice). The 2760 must then be manually reset by depressing the RESET MAN switch to clear the hard latch state and resume normal operation. Table I provides the general functions of the KEYPAD keys for programming operations.

4.31 Fig. 10 illustrates in a flowchart the responses of the 2760 to various keying sequences. The parallelogram symbol indicates that the 2760 is waiting for a character to be keyed in.

4.32 The diamond symbols show the questions asked by the 2760 about the keyed character. The 2760 must determine which character has been entered in order to proceed. Although all 16 keys are used, not all the keys are valid at all times. The 2760 simply ignores an invalid entry and waits for another character.

4.33 A rectangle symbol describes the action in response to a keypad entry. Most of the time, the action is visually apparent to the user. In some instances, no visual evidence of the response is given. For example, if two characters are required to complete an instruction then there is no visual response between the entries. Also, displaying an empty memory on a cleared display gives no visual evidence that an action has taken place. In these cases, the user must proceed with the next entry. If an expected visual response does not occur then probably an invalid character was keyed in. The 2760 will ignore the invalid character and wait for a new character.

TABLE I

KEYPAD KEY FUNCTIONS

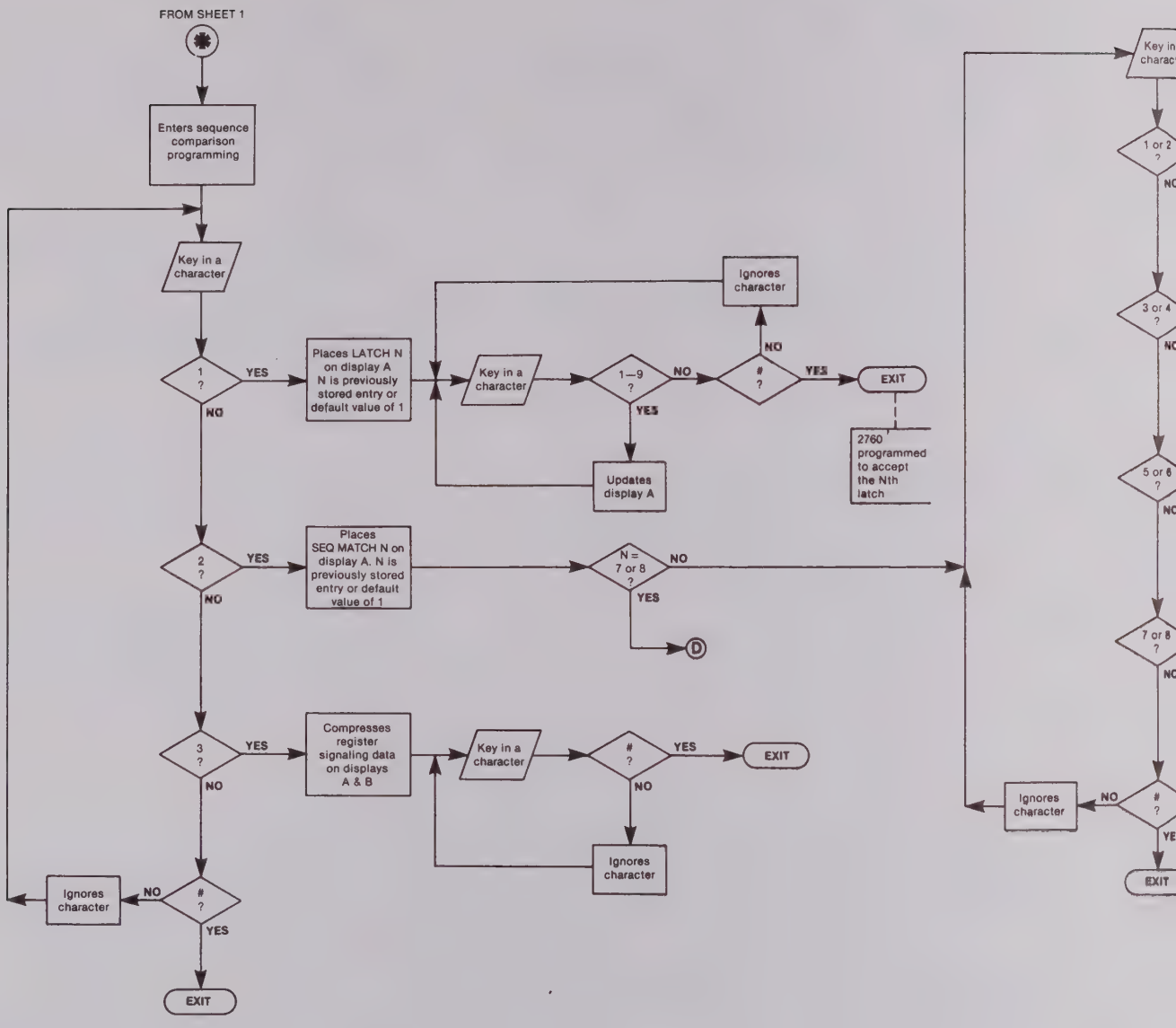
KEY(S)	DESCRIPTION
*	Enters mainframe program mode
0-9	Enters digits 0 to 9
AO-A9	Accesses one of ten files in the comparison memory. A0 for file 1, A1 for file 2, etc.
B1	Accesses latch selection program
B2	Accesses match selection program
B277	Accesses reformat program
B288	Accesses reformat program
B3	Accesses compressed display program
C	Erases entered time of day or erases the selected comparison memory file
D	Accesses time of day program
*1 – *9	Enters codes 11-19 into a comparison memory file
**	Enters a wild card into a comparison memory file
#	Exits mainframe program mode

REFORMAT PROGRAM CODES

KEY	DESCRIPTION	
A	Accept digit	A on display
B	Fill with wild card	F on display
C	Delete last code entered	
D	Delete digit/code at this location	d on display
*	Replace with wild card	c on display

Notes:

1. REFORMAT PROGRAM CODES are entered after the reformat program is accessed.
2. B1 means key in B and then 1.
3. B288 means key in B, then 2, then 8, and then 8 again.


FROM SHEET 1
Enters sequence comparison programming
Key in a character
1 ?
YES
NO
Places LATCH N on display A N is previously stored entry or default value of 1
Key in a character
1—9 ?
NO
YES
Updates display A
#
?
NO
YES
Ignores character
EXIT
2760 programmed to accept the Nth latch
2 ?
YES
NO
Places SEQ MATCH N on display A. N is previously stored entry or default value of 1
N = 7 or 8 ?
NO
YES
D
3 ?
YES
NO
Compresses register signaling data on displays A & B
Key in a character
#
?
YES
NO
EXIT
Ignores character
#
?
NO
YES
Ignores character
EXIT
Key in
charac
1 or 2
?
NO
3 or 4
?
NO
5 or 6
?
NO
7 or 8
?
NO
Ignores character
NO
#
?
YE
EXIT

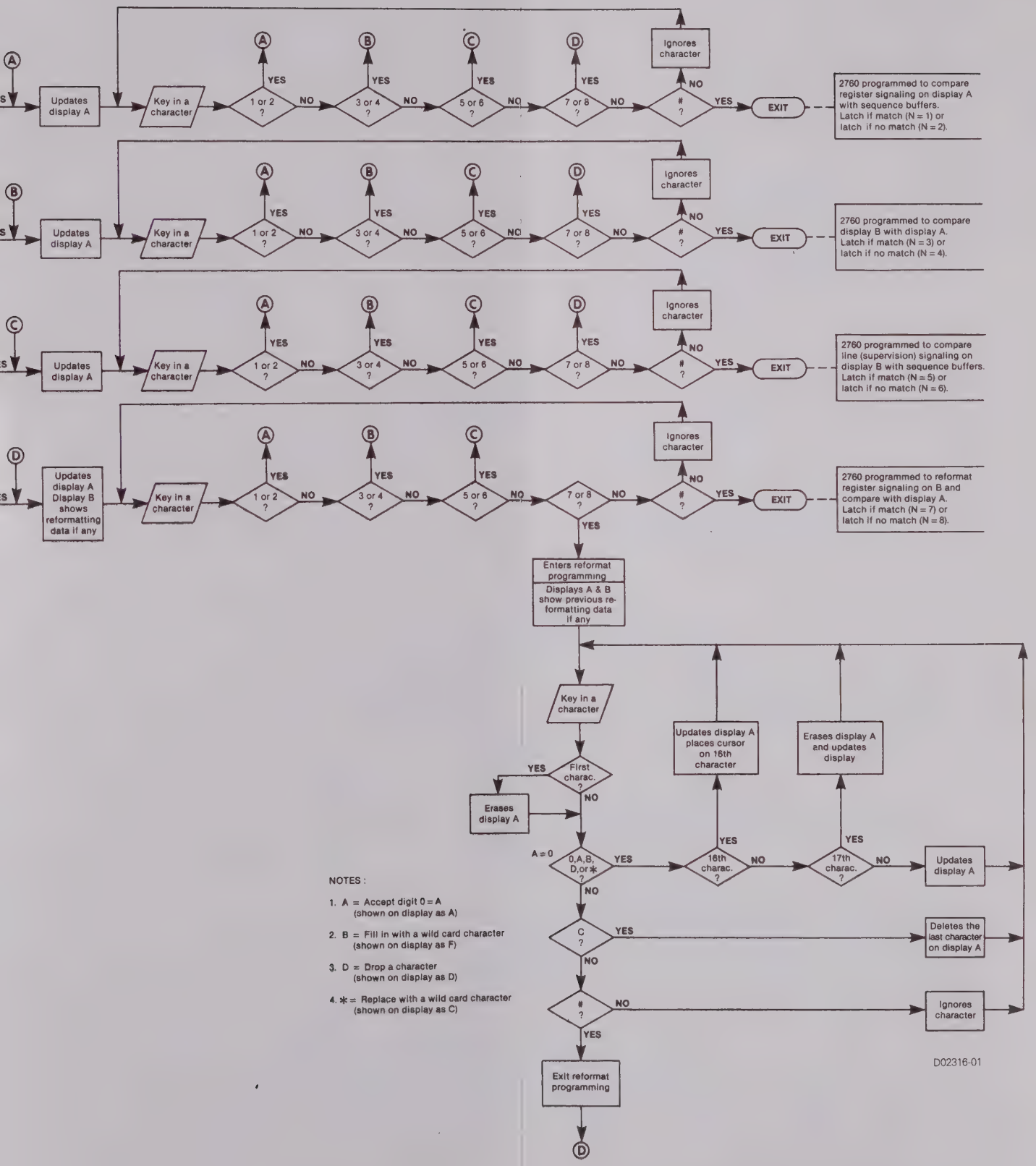

A
Updates display A
Key in a character
1 or 2 ?
3 or 4 ?
5 or 6 ?
7 or 8 ?
?
YES
NO
Ignores character
EXIT
2760 programmed to compare register signaling on display A with sequence buffers. Latch if match (N = 1) or latch if no match (N = 2).
B
Updates display A
Key in a character
Ignores character
EXIT
2760 programmed to compare display B with display A. Latch if match (N = 3) or latch if no match (N = 4).
C
Updates display A
Key in a character
Ignores character
EXIT
2760 programmed to compare line (supervision) signaling on display B with sequence buffers. Latch if match (N = 5) or latch if no match (N = 6).
D
Updates display A Display B shows reformatting data if any
Key in a character
Ignores character
EXIT
2760 programmed to reformat register signaling on B and compare with display A. Latch if match (N = 7) or latch if no match (N = 8).
Enters reformat programming
Displays A & B show previous re-formatting data if any
Key in a character
First charac. ?
Erases display A
Updates display A places cursor on 16th character
Erases display A and updates display
A = 0
0,A,B, D,or * ?
16th charac. ?
17th charac. ?
Updates display A
C ?
Deletes the last character on display A
?
Ignores character
Exit reformat programming
NOTES :
1. A = Accept digit 0 = A (shown on display as A)
2. B = Fill in with a wild card character (shown on display as F)
3. D = Drop a character (shown on display as D)
4. * = Replace with a wild card character (shown on display as C)
D02316-01

Fig. 10—Keypad Programming Flowchart (Sheet 2 of 2)

TABLE K

TIME OF DAY PROGRAMMING EXAMPLE

KEYS	DISPLAY B	REMARKS
*	previous	Enters keypad programming and places the 2760 in a hard latch state.
D	000000	Specifies time of day program.
05268	052680	Display B updated as each digit is entered. 5:26:80 entered as the time of day in hours:minutes:seconds format.
C	000000	C key clears time of day; incorrect time of day entered.
0526	052600	5:26:00 entered as the time of day.
#	052600	Display B shows the entered time of day. Updated time shown on display B if RCL SUPV switch is pressed. Press MAN RESET to release the hard latch.
The sequence consisting of *, D, # resets the system time to zero. The system time then shows the elapsed time since the clock reset occurred.		

H. Comparison Memory Programming

4.36 The Model 2760 may be programmed or instructed to look for a particular called number or series of supervision events occurring in monitored traffic. To accomplish this the called number(s) or supervision events series are stored in the comparison memory.

4.37 Either register or line signaling sequences to be compared are entered via the 2760's KEYPAD. These sequences are stored in a comparison memory. The comparison memory is partitioned into 10 files (0 through 9). Thus, the comparison memory can hold up to 10 individual signaling sequences. Each file may contain a sequence of up to 16 digits and/or codes representing an address (a station number) or portion of an address. The stored digits and codes can also represent a supervision signaling sequence or portion of a supervision signaling sequence.

4.38 The Lead Digit Ident display identifies the number of the next digit to be entered. When the sixteenth digit or code is keyed in, a copy of the digits entered on display A appears on display B and the last digit in the dual display blinks. (CURSOR). Keying a seventeenth digit or code causes the first 16 digits/codes on display A to be erased and the seventeenth digit or code becomes the new first digit or code for that comparison file.

4.39 Table L describes the functions of the KEYPAD keys for comparison programming. Table M shows examples of comparison programming. Table M consists of eight parts as follows:

Part 1: A power up reset erases all comparison files.

Part 2: Wild cards 603 placed in file 0.

Part 3: Wild cards 218 placed in file 1.

Part 4: Wild cards 219 placed in file 2 in error. Error corrected.

Part 5: Change file 1 contents (method 1).

Part 6: Change file 1 contents (method 2).

Part 7: Empty file 2.

Part 8: Review contents of file 0.

4.40 For comparison memory programming practice, execute parts 1-8 in order, part 1 first, then part 2 etc. After each step the RESET MAN switch must be depressed to clear the hard latch state.

TABLE L

COMPARISON PROGRAMMING KEYS

KEYS	DISPLAY A	DISPLAY B	REMARKS
*	previous	previous	Accesses keypad programming and places the 2760 in a hard latch state.
A, 0 to A, 9	notes 1, 2	note 1	Specifies one of ten files in the sequence comparison memory buffer.
* *	c	note 1	Signifies a wild card used for sequence comparison. Any character matches the wild card.
0 to 9	0 to 9	note 1	Digits used for sequence comparison.
*, 1 to *, 9	•1 to •9	note 1	Codes used for sequence comparison.
C	blank	note 1	Erases the selected sequence comparison file.
#	previously entered digits or codes	previously entered digits or codes	Exits keypad programming. Press MAN RESET to release the hard latch. Refer to note 3.

Notes:

1. If the selected sequence comparison file has been programmed since the last power-up reset then displays A and B show the contents of the selected sequence comparison file. Display A is updated as the digits and/or codes are entered. Display B is updated when the # key is pressed.

2. After keying *A, the keypad program ignores keying of A, B, and D.

3. After keying #, the dual display returns the same data it had prior to entering keypad programming. That is, the display should show line signaling and system time if RCL SUPV switch was set at the time keypad programming was entered. Previously stored register signaling, if any, returns on the display if RCL SUPV switch was not set.

TABLE M

COMPARISON PROGRAMMING EXAMPLES

KEYS OR SIGNAL	DISPLAY A	DISPLAY B	REMARKS
1.			
Power-up	blank	blank	All comparison files are erased.
2.			
*	blank	blank	Enters keypad programming.
A0	blank	blank	Accesses comparison file 0
* * 603	c603	blank	Programs "wild card", 6, 0, 3 in file 0. Display A updated as each digit or code is entered.
#	c603	c603	Exits keypad programming. Display B shows the contents of file 0.
3.			
*	blank	blank	Enters keypad programming.
A1	blank	blank	Accesses comparison file 1.
* * 218	c218	blank	Programs "wild card", 2, 1, 8 in file 1. Display A updated as each digit or code is entered.
#	c218	c218	Exits keypad programming. Display B shows the contents of file 1.
4.			
*	blank	blank	Enters keypad programming.
A2	blank	blank	Accesses comparison file 2.
* * 219	c219	blank	Programs "wild card", 2, 1, 9 in file 2. Display A updated as each digit or code is entered.
C	blank	blank	C key erases contents of file 2. Sequence C219 was not the desired comparison.
* * 229	c229	blank	Programs "wild card", 2, 2, 9 in file 2. Display A updated as each digit or code is entered.
#	c229	c229	Exits keypad programming. Display B shows the contents of file 2.

TABLE M (Cont)

KEYS OR SIGNAL	DISPLAY A	DISPLAY B	REMARKS
5.			
*	blank	blank	Enters keypad programming mode.
A1	c218	c218	Accesses comparison file 1. Display A and B show the contents of file 1.
* * 216	c216	c218	Reprograms "wild card", 2, 1, 6 in file 2. Display A updated as each digit or code is entered.
#	c216	c216	Exits keypad programming. Display B shows the contents of file 1. File 1 contents have changed from c218 to c216.
6.			
*	blank	blank	Enters keypad programming.
A1	c216	c216	Accesses comparison file 1. Display A and B show the contents of file 1.
C	blank	c216	The C key erases contents of file 1.
* * 601	c601	c216	Reprograms "wild card", 6, 0, 1 in file 2.Display A updated as each digit or code is entered.
#	c601	c601	Exits keypad programming. Display B shows the contents of file 1. File 1 contents have changed from c216 to c601.
7.			
*	blank	blank	Enters keypad programming.
A2	c229	c229	Accesses comparison file 2. Displays A and B show the contents of file 2.
C	blank	c229	C key erases contents of line 2.
#	blank	blank	Exits keypad programming. File 2 content has been deleted.
8.			
*	blank	blank	Enters keypad programming.
A0	c603	c603	Accesses comparison file 0.
#	c603	c603	Exits keypad programming.

4.41 Wild Card

4.42 A wild card digit placed in a comparison memory file is like a wild card in a card game. It is a "universal match" type of digit. The Model 2760 accepts as a valid match any digit/code of a monitored call which coincides with the wild card position or location in the memory file. Some examples may help to make this clear.

4.43 In the following examples:

C (Call) = Sequence of digits in monitored call
M (Memory) = Sequence of digits stored in memory file
c = Wild card position

C 612 545 6103	No match exists
M 612 546 6103	No wild card positions in memory 5 does not match 6
C 612 545 6103	Match exists
M 612 545 61cc	cc are wild card positions o matches c 3 matches c
C 612 545 6103	Match exists
M CCC 545-6103	6 matches c 1 matches c 2 matches c
C 218 739 1234	No match exists
M 218 74c 1234	3 does not match 4 9 matches c

4.44 A small lowercase letter c is used on the displays to indicate a wild card position ("c" for card). Monitored digits/codes are considered wild if they occur opposite a "c" stored in memory. In other words they occupy the same position in the sequence of digit/codes as a c stored in a comparison memory file.

4.45 Note that it is necessary to enter and then exit keypad programming for each comparison file accessed. When comparison programming or reviewing is finished the RESET MAN switch must be momentarily depressed to remove the 2760 from the hard latch state.

I. Latch States and Resets

4.46 A "latch" (or hold condition) may be caused by an operator action or requested by a plug-in module. A lighted LATCH indicator shows that a latch state exists. Also, at the beginning of a latch, a 256 to 512-millisecond tip/ring closure appears at the LATCH output port.

4.47 Latches are classified either as hard or soft latches. A hard latch can only be cleared by a manual reset (RESET MAN switch) or by a remote reset applied at the RESET REM port. Soft latches may be cleared by a plug-in module without operator intervention. A soft latch may also be cleared by a manual or a remote reset.

4.48 Operator actions that cause hard latches are:

(1) Entering mainframe instructions into the 2760 (using the keypad).

(2) Scanning the register (address) signaling data on the dual display using either the left or right CURSOR switches.

(3) A hard latch is also caused when a register (address) signaling memory fills up and the NO ERASE switch is set.

4.49 During operator-caused latches, all plug-in modules are inhibited and the monitoring of register and line signaling stops. The contents of the register (address) signaling and supervision memories remain unchanged for the duration of a latch. Therefore, the previously stored signaling can be reviewed at the operator's convenience.

4.50 The 2760 may be programmed to acknowledge only the Nth latch request from enabled plug-in modules. That is, the 2760 does not enter into a soft latch state until a specified number (1 to 9, defaults to 1) of latch requests have been received from any of the enabled plug modules.

4.51 Once in the soft latch state, the 2760 sends the contents of displays A and B register (address) signaling memories to a printer output port. Refer to Part 3 for a description of the Model 2760-21 Printer Control Module. The 2760 then does a sequence comparison as programmed.

4.52 The soft latch state remains until either it is changed into a hard latch or is reset. The 2760 changed the soft latch into a hard latch if one of the following conditions exists:

(1) A soft latch state exists and the RESET AUTO switch is not depressed.

(2) A soft latch state exists, a signal error was detected, and the HOLD ERROR switch is depressed.

(3) A soft latch state exists, a sequence match is subsequently detected, and the HOLD MATCH switch is depressed.

4.53 When a soft latch from a register address signaling plug-in module becomes a hard latch, the register address signaling plug-in module cannot supply digits/codes to the register (address) signaling memory. However, the line signaling (supervision) monitoring continues until an "idle" supervision condition is detected.

4.54 Table N lists the latch and reset conditions associated with the mainframe. Refer to the individual module instruction manuals for definitions of their latch signals and automatic resets.

TABLE N

LATCHES AND RESETS

LATCH	CONTROL	TYPE OF LATCH	RESET
1. power off	POWER	hard	Pwr
2. scroll/cursor		hard	Man or Rem
3. sequence comparison	* key	hard	# (number) key and MAN or Rem
4. sequence match	HOLD MATCH off	note 2	Auto, Man, or Rem
sequence match	HOLD MATCH on	note 3	Man or Rem
5. signal error	HOLD ERROR off	note 2	Auto, Man, or Rem
signal error memory	HOLD ERROR on	note 3	Man or Rem
6. register data full	NO ERASE on	hard	Man or Rem
7. program error	module ENABLE	hard	Correcting the module enable programming
8. module latches	module ENABLE and AUTO RESET on	soft if no sequence match and/or signal error (refer to 4 and 5)	Auto, Man, or Rem
9. module latches	module ENABLE and AUTO RESET off	note 3	Man or Rem

Man = manual reset; Rem = remote reset; Pwr = power-up reset; Auto = automatic reset

Notes:

1. Power-up reset erases the contents of all memories (data, supervision, sequence comparison, etc.).
2. Soft latch caused by end of signaling remains soft.
3. Soft latch caused by end of signaling changes into a hard latch.

J. Latch Selection Programming

4.55 Latch selection allows the operator to specify which latch request from a plug-in module to acknowledge. If the request is acknowledged, the instrument enters a soft latch state.

4.56 The Model 2760 may be programmed to acknowledge any plug-in module latch request from the first to the ninth. To access latch selection programming simply key in (*) (B) (1). (See Fig. 10.) Then key in any desired latch request number (1 to 9). Key in (#) to exit KEYPAD programming. Depress RESET MAN to clear hard latch. Table O describes the functions of the KEYPAD keys for latch selection programming.

4.57 At power up the Model 2760 is always initially set to acknowledge the first latch request from a plug-in module. Refer to the instruction manuals of the individual modules for definitions of their latch requests and automatic resets.

TABLE O

LATCH SELECTION PROGRAMMING

KEYS	DISPLAY A	DISPLAY B	REMARKS
*	previous	previous	Accessed keypad programming and places the 2760 in a hard latch state.
B1	LATCHn (notes)	blank	Specifies latch selection program.
1 to 9	LATCHm (notes)	blank	Digits used to specify which latch the 2760 should recognize.
#	previous	previous	Exits keypad programming. Press MAN RESET to release the hard latch.

Notes:

1. After keying *B, the keypad program accepts only 1, 2, 3, or #.
2. After keying *B1, the keypad program accepts only digits 1 through 9 and #.
3. n default value of 1 or last stored value.
4. m last valid keyed in value.

K. Sequence Comparison

4.58 After entering a soft latch state, the 2760 compares (as programmed):

(1) Edited register signaling from the Display A memory with pre-selected signaling sequences stored in a comparison memory, or

(2) Edited register signaling from the Display A memory with the edited register signaling from the Display B memory, or

(3) Edited register signaling from the Display A memory with the edited and reformatted register signaling from the Display B memory, or

(4) Edited line signaling from the supervision memory with pre-selected supervision sequences stored in the comparison memory.

4.59 The 2760 may also be instructed to change the soft latch into a hard latch if:

(1) The HOLD MATCH switch is depressed and

(2) A match is either found or not found.

4.60 The Model 2760 may therefore be programmed to hard latch on any one of eight different conditions. For each of the four types of comparisons a match is either found or not found, thus there are eight separate possibilities.

4.61 Prior to a sequence comparison, the 2760 edits either the contents of the Display A memory or of the supervision memory and stores the edited data in a sequence memory. Editing consists of deleting error codes (-), brackets (I,I), and data between the brackets. Up to 16 signal digits/codes may be stored in the sequence memory. If a comparison is made with the data of Display B memory, then the Display B memory is also similarly edited. The edited contents of the Display B memory may require reformatting.

4.62 If a specified match condition is found during a sequence comparison, the contents of the sequence memory is sent to the printer output port. In addition, the soft latch changes into a hard latch if the HOLD MATCH switch is depressed.

L. Sequence Match Selection Programming

4.63 As described previously, the operator may select the type of sequence comparison the 2760 should do. Register signaling sequence comparison occurs when the 2760 enters a soft latch state and line signaling sequence comparison takes place when the monitored circuit goes idle or the soft latch is reset either manually or remotely.

4.64 To access latch selection programming, key in (*) (B) (2). (See Fig. 10.) Table P describes the KEYPAD keys as they relate to the sequence match selection programming. At power up, the 2760 is always initially set for sequence match 1 to compare the edited Display A memory with register signaling sequences stored in the comparison memory. It will change the soft latch into a hard latch if a match is found and the HOLD MATCH switch is depressed.

TABLE P

SEQUENCE MATCH SELECTION PROGRAMMING

KEYS	DISPLAY A	DISPLAY B	REMARKS
*	previous	previous	Accesses keypad programming and places the 2760 in a hard latch state.
B2	SEQ MATCHn (notes)	blank or previous reformat data if n equals 7 or 8	Specifies match selection program.
1 to 8	SEQ MATCHm (notes)	blank or previous reformat data if m equals 7 or 8	Digits used to select the sequence matched conditions. ***Note:*** Latching occurs only if the specified match condition exists and HOLD on MATCH control is set. 1. latch if the edited DISPLAY A memory matches one of the pre-selected register signaling sequences stored in the comparison memory. 2. latch if the edited DISPLAY A memory does not match any of the pre-selected register signaling sequences stored in the comparison memory. 3. latch if the edited DISPLAY A memory matches the edited DISPLAY B memory. 4. latch if the edited DISPLAY A memory does not match the edited DISPLAY B memory. 5. latch if the edited supervision memory matches one of the pre-selected line signaling sequences stored in the comparison memory.

TABLE P (Cont)

KEYS	DISPLAY A	DISPLAY B	REMARKS
1 to 8 (Cont)	SEQ MATCHm (notes) (Cont)	blank or previous reformat data if m equals 7 or 8 (Cont)	6. latch if the edited supervision memory does not match any of the pre-selected line signaling sequences stored in the comparison memory. 7. latch if the edited DISPLAY A memory matches the edited and reformatted DISPLAY B memory. 8. latch if the edited DISPLAY A memory does not match the edited and reformatted DISPLAY B memory.
#	previous	previous	Exits keypad programming. Press MAN RESET to release the hard latch.

Notes:

1. After keying *B, the keypad program accepts only 1, 2, 3, or #.
2. After keying *B1, the keypad program accepts only digits 1 through 8 and #.
3. n defaults value of 1 or last stored value. If n equals 7 or 8, refer to Table P or DISPLAY B memory reformat program.
4. m last valid keyed in value. If m equals 7 or 8, refer to Table P for DISPLAY B memory reformat program.

M. Input/Output Comparison

4.65 The Model 2760 permits easy one-for-one digit comparisons to be made between the inputs and outputs of dial pulse repeaters, translators, converters, and similar equipment used in various signaling arrangements. For translators and converters, where the input and output signaling formats are different, means have been provided to change either format so a direct comparison may be made.

N. DISPLAY B Memory Reformat Programming

4.66 Sequence match 7 or sequence match 8 allows comparing two register (address) signaling sequences with different format such as where signal codes have been added and/or dropped. For example: a dial pulse to MF converter adds the KP and ST codes to the digits.

4.67 To properly program in the reformat instructions, it is essential that the formats of the two signaling sequences be known. Reformatting is done only on the data stored in the DISPLAY B memory and not on the data stored in the DISPLAY A memory. Thus, it is necessary to change the format in the DISPLAY B memory to obtain the same format as the signaling stored in the DISPLAY A memory.

4.68 Each of the reformatting instructions are entered into the 2760 as single key entries. The reformatting instructions are:

(1) Accept the digit or code as is . . . key A (shown on the display as R)

(2) Insert a wild card character . . . key B (shown on the display as F)

(3) Delete the digit or code and close up the gap . . . key D (shown on the display as d)

(4) Replace the digit or code with a wild card character . . . key *(shown on the display as c).

4.69 The C key functions as an editing key. Each time the C key is pressed the last valid reformat instruction is deleted. In this way, an incorrect entry can be taken out and a new instruction entered.

4.70 As reformat instructions are keyed in, the codes for these instructions appear on DISPLAY A. DISPLAY B shows previously stored reformat instructions if any. Up to 16 instructions can be stored. On the 16th entry, the blinking CURSOR is

placed over the last entry. The blinking CURSOR informs the operator that the maximum number of reformat instructions have been entered. If a 17th entry is keyed in then DISPLAY A is erased and the last entry becomes the first.

4.71 Table Q summarizes the functions of the keypad keys as they relate to reformat instructions. To access reformat instructions programming, key in *B27 (*)(B)(2)(7) or (*)(B)(2)(8). (See Fig. 10.) Note that it is necessary to first enter the sequence match selection program to reach the reformat instructions programming . . . reformat instructions programming is a subroutine of the sequence match selection programming. The # key causes an exit from the reformat instructions programming and returns the user to the sequence match selection programming.

4.72 Figures 11 and 12 illustrate the use of reformat instructions to change the format of the data stored in the DISPLAY B memory to conform with the data stored in the DISPLAY A memory. Note that the editing and reformatting are internally done and that the appearances of the displays do not change when editing, reformatting, and comparing takes place.

4.73 In the example of Fig. 11, the MF signaling is stored in DISPLAY B memory, whereas dial pulsing is stored in DISPLAY B memory for the example of Fig. 12. Different instructions (although similar) are required to change the data format of DISPLAY B memory. In one case a character is deleted and in the other case, a wild character is inserted.

TABLE Q

DISPLAY B MEMORY REFORMAT PROGRAMMING

KEYS	DISPLAY A	DISPLAY B	REMARKS
*B27 or *B28	SEQ MATCHn (n = 7 or 8)	Previous reformat data if any	
1, 6	SEQ MATCHm	blank	Returns to sequence match selection. Refer to Table P.
7, 8	Previous reformat data if any	Previous reformat data if any	Accesses reformat programming.
0, A, B, C, D, *	Updated reformat data	Previous reformat data if any	0, A (F) - accept the digit or code as is at this location, B (F) - shift remaining codes to the right and insert a wild card character at this location, C - delete the last valid reformat instruction entered, D (d) - delete the digit or code at this location, * (c) - replace the digit or code at this location with a wild card character.
#	SEQ MATCHm	Updated reformat data if any	If in reformat data programming, return to sequence match selection. If in sequence match selection, exit keypad programming.

Notes:

1. In the reformat data programming, the keypad program accepts only 0, A, B, C, D, and * keys and ignores all other keys.

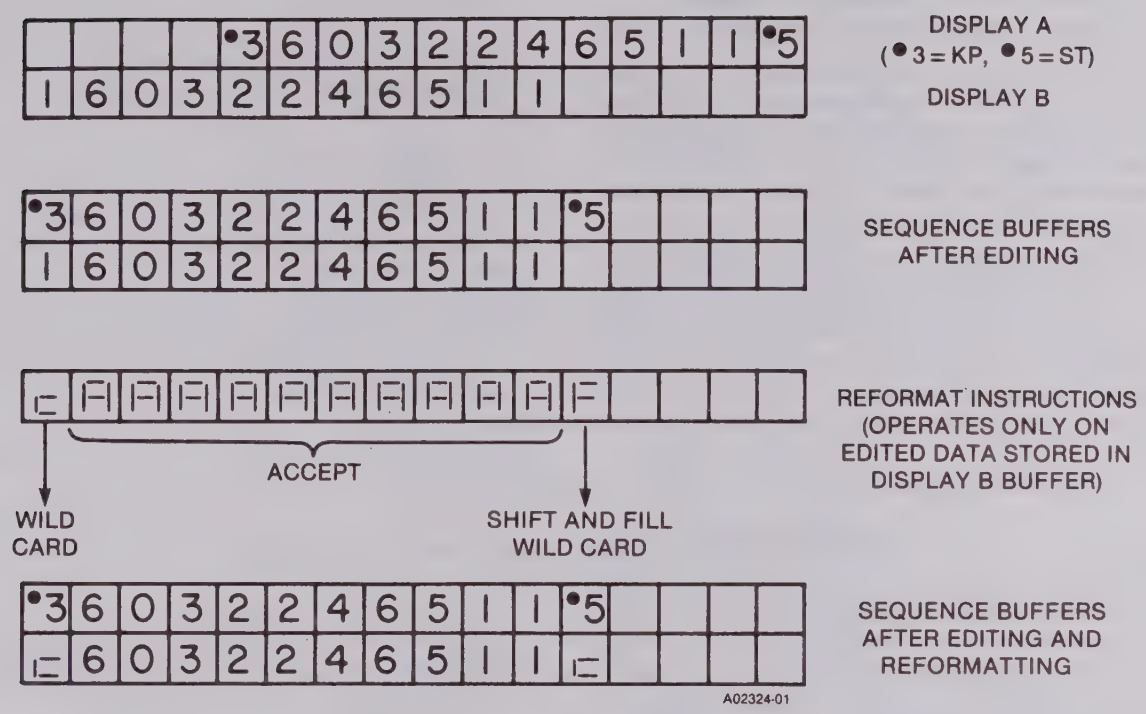


Fig. 11—Example of Reformat Instructions for Dial Pulsing on DISPLAY A and MF Signaling on DISPLAY B

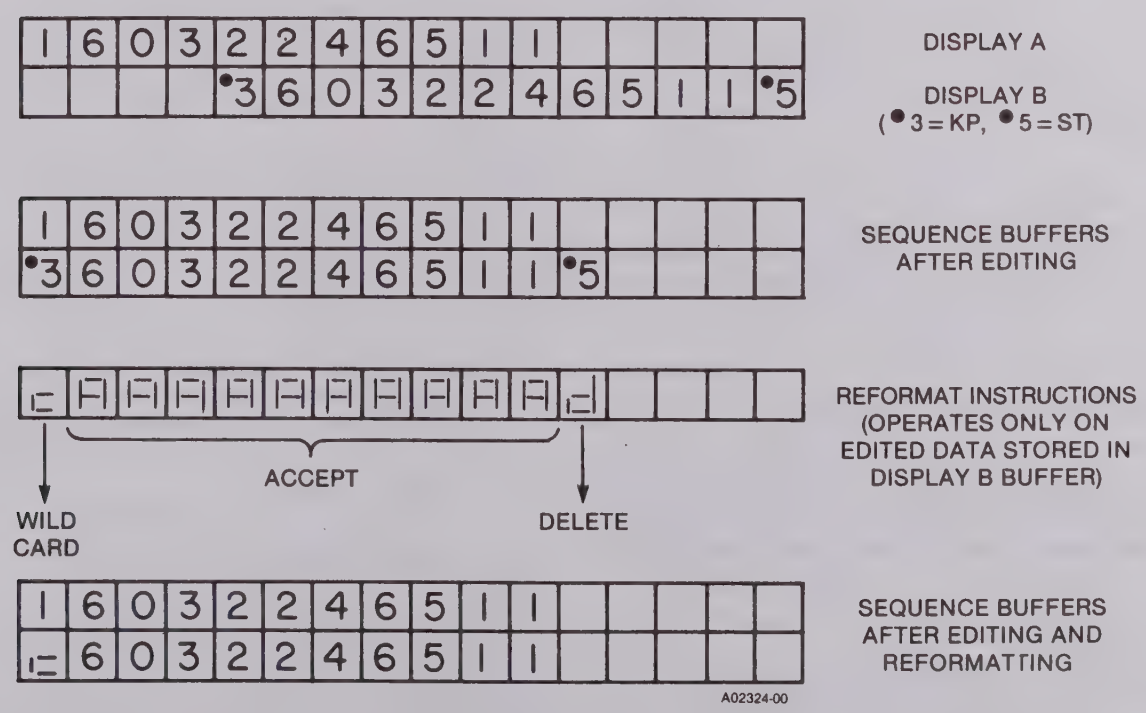


Fig. 12—Example of Reformat Instructions for MF Signaling on DISPLAY A and Dial Pulsing on DISPLAY B

O. Modes 2 and 3 Compressed Display Programming Register (Address) Signaling

4.74 When reviewing register (address) signaling in display mode 2 or 3, the operator may instruct the Model 2760 to remove all brackets and the data between the brackets from the A and B DISPLAYS. The displayed data is compressed to fill the space that was occupied by the deleted brackets and data.

4.75 The deleted data is not lost since it remains within the A and B DISPLAY memories. It is simply not shown on the A and B displays. This feature allows the operator to view the first 16 register (address) signaling digits/codes as a single group when in mode 2 or 3.

4.76 Enter (*) (B) (3) on the KEYPAD to compress the register (address) signaling on DISPLAYS A and B. Keying in (#) returns DISPLAYS A and B to their normal mode 2 or 3 presentation.

4.77 Table R shows an example of compressed display programming. Notice that only the first 16 register (address) signaling digits/codes and errors (-) may be reviewed in a compressed display. Any additional register (address) signaling codes/digits stored in memory must be reviewed in the normal manner by scanning with the CURSOR switches. A mode 3 compressed display will contain a maximum of only 15 digits/codes.

TABLE R

COMPRESSED DISPLAY PROGRAMMING EXAMPLE

KEYS	DISPLAY A	DISPLAY B	REMARKS
*	uncompressed data	uncompressed data	Accesses keypad programming and places the 2760 in a hard latch state. (Refer to note 1.)
B3 (notes)	compressed data	compressed data	Displays the first 16 register signaling codes stored in the display buffers. (Refer to notes 2 and 3.)
#	uncompressed data	uncompressed data	Returns the display to its previous mode and exits keypad programming. Press MAN RESET to release the hard latch.

Notes:

1. A compressed display is normally programmed after register signaling has been monitored and codes stored.
2. While in the compressed display mode, the 2760 cannot do anything else.
3. After keying * B3, the keypad program ignores all keys except the # key.

4.78 Line (Supervision) Signaling

4.79 Depending on the enabled plug-in module the supervision display (DISPLAY A) may appear in either mode 1 or mode 2. Compressed mode 2 supervision displays are not possible. Mode 3 displays are not provided for supervision plug-in modules.

P. Display Interpretation

4.80 In order to interpret the significance of any particular DISPLAY A or B presentation it is essential to understand:

- Displays
- Display Modes
- Display Symbols and Characters
- Display Blanks.

These items are discussed in the paragraphs which follow.

4.81 Displays

4.82 The display area consists of two rows of 16 characters each (including blanks). The top row is DISPLAY A. The bottom row is DISPLAY B.

4.83 The data shown on the A and B DISPLAYS appears either in real time or in recall.

4.84 In real time, DISPLAYS A and B show register (address) signaling as received. DISPLAY A can also show line signaling (supervision events) in real time while DISPLAY B shows the system time.

4.85 In recall, the A and B DISPLAYS can present several types of data that were previously stored in memory.

4.86 Display Modes

4.87 Display modes are described in detail in paragraphs 3.30 to 3.44. Examples of display modes are shown in Fig. 6.

4.88 There are three different display modes used. The three modes are:

- Dialed Number Display
- Violation and Error Display
- Measure Display.

4.89 The operator and the plug-in module determine the display mode. The various modules provide for one, two, or three different modes. Line (supervision) signaling plug-in modules do not provide a mode 3 display.

4.90 The operator selects the display mode by programming or instructing the plug-in module to use one of its available modes. This is accomplished by keying in the appropriate instructions by means of the KEYPAD.

4.91 Mode 1 Display

4.92 In mode 1, the display shows the digits/codes for all signals which fall within preset MIN and MAX parameter limits. A dash (-) represents an error or a signal which does not contain the correct number of frequencies or does not have the proper number of pulses.

4.93 Mode 2 Display

4.94 In mode 2, the display shows the digits/codes for signals and errors as in mode 1. For signals with one or more parameters falling outside the programmed lower and upper limits, the display shows codes enclosed between brackets for gap (interval between the current signal and the previous signal), pulse width, and signal level. Thus bracket information is referred to as the "GPL" data. The SIG ERR indicator flashes on and off to alert the operator that the stored call has an error or violation. See Fig. 13.

4.95 For a signal with an error, the display shows codes which identify the frequencies or tones present in the pulse along with the GPL codes. Refer to individual plug-in module manuals for code definitions pertaining to frequency and pulse contents.

4.96 Mode 3 Display

4.97 In mode 3 the display shows the measured values for gap, pulse width, and level for each signal (or error) received. As shown in Fig. 14, these signal values are placed between two brackets and a full 16-slot display is required. Mode 3 therefore is available only for a few register signaling receiver modules . . . Model 2760-11 DTMF Register Receiver, Model 2760-13 MF Register Receiver, and Model 2760-14 CCITT No. 5 Register Receiver.

> ***Note:*** To ensure the accuracy of measured signal values, it is important that only one of two possible enabled register signaling receivers be programmed for mode 3 operation at any one time.

4.98 The user can recall the programmed parameters of an enabled plug-in module by momentarily pressing the module's PROGRAM switch. The data stored in the DISPLAY A and B memories and supervision memory is not lost if no module ENABLE is released and the mainframe RESET MAN switch is not depressed. This feature allows comparing the measured parameters with the programmed limits for that signal.

4.99 In mode 3 the SIG ERR indicator flashes on and off only for errors and not for violations. Also, for errors, the frequencies or tones present in the pulse are not shown.

4.100 Display Digits, Letters, and Symbols

4.101 Figure 15 shows digits and symbols and Fig. 16 shows letters and symbols used for the various displays.

S [GPL]
or −(GPLc]

S = signal code

− = error . . . not two and only two frequencies present or incorrect number of pulses

G = gap

P = pulse width

L = pulse level

C = one for each frequency or pulse present

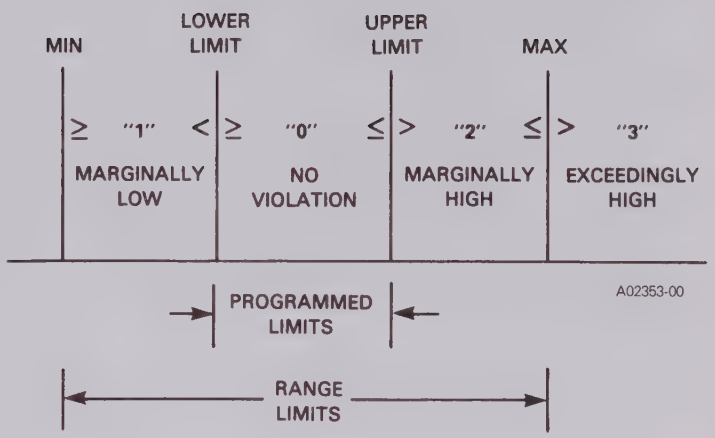
For G, P, L

0 = no violation . . . between or equal to the programmed upper and lower limits

1 = marginally low . . . less than the programmed lower limit and greater than or equal to the minimum range value

2 = marginally high . . . greater than the programmed upper limit and less than or equal to the maximum range value

3 = exceedingly high . . . greater than the maximum range value



NOTE

SIG ERR indicator flashes on and off to alert the operator that the call had an error or violation.

Fig. 13—Definitions of Error and Violation Terms

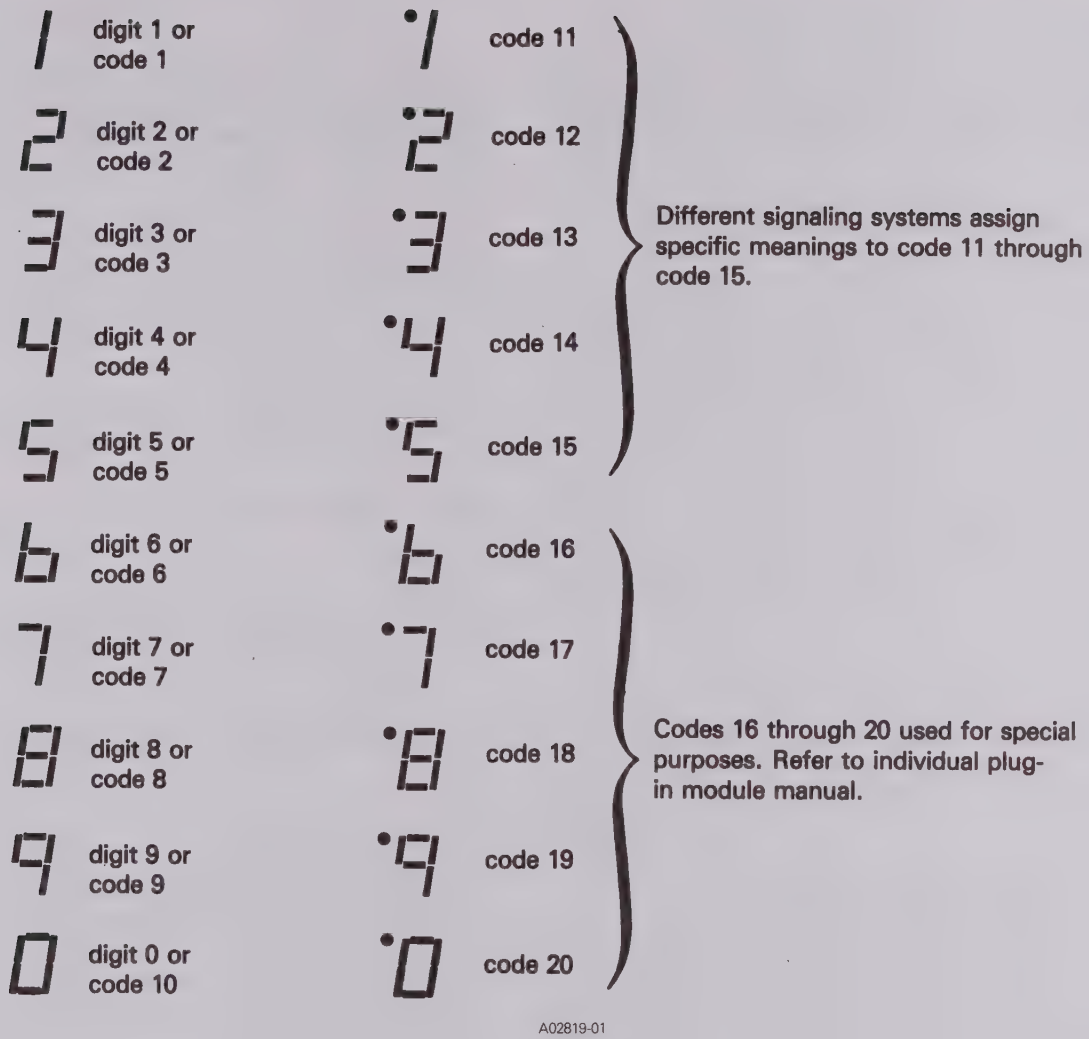
S = signal code or error

GGGG = gap in milliseconds

PPPP = pulse width in milliseconds

LLL = level in dBm . . . negative value shown with minus (−) sign, positive value without a plus sign.

Fig. 14—Mode 3 Format


digit 1 or code 1
code 11
digit 2 or code 2
code 12
digit 3 or code 3
code 13
Different signaling systems assign specific meanings to code 11 through code 15.
digit 4 or code 4
code 14
digit 5 or code 5
code 15
digit 6 or code 6
code 16
digit 7 or code 7
code 17
digit 8 or code 8
code 18
Codes 16 through 20 used for special purposes. Refer to individual plug-in module manual.
digit 9 or code 9
code 19
digit 0 or code 10
code 20
A02819-01

(blank) a blank may indicate:
1. signal did not meet minimum tone duration,
2. signal level was overrange,
3. separation between two calls in "no erase" mode display,
4. two signals arrived sequentially on the other display

upper dash — symbol for MF2 signaling forward prefix (code 14)

lower dash — symbol for MF signaling backward prefix (code 9)

dash — indicates error in a multifrequency signal - signal did not have two and only two frequencies

wild card — used in sequence comparison programming

Fig. 15—Display Digits and Symbols

DISPLAY	LETTER	DISPLAY	SYMBOL
A	A	[	[
F	B	]	]
C	C	c	*
d	D		
E	E		
	F		
	G		
H	H		
I	I		
	J		
	K		
L	L		
r n	M		
	N		
	O		
P	P		
q	Q		
r	R		
S	S		
t	T		
U	U		
	V		
	W		
	X		
y	Y		
	Z		

A02819-02

Fig. 16—Display Letters and Symbols

4.102 Display Blanks

4.103 A blank space between received register (address) signaling digits/codes on either DISPLAY A or B may have any one of four different meanings. Blanks between register (address) signals are used to:

(1) Separate sets of register (address) signaling digits/codes from different calls. The NO ERASE and RESET AUTO switches must be depressed.

(2) Indicate a signal did not meet the minimum tone duration.

(3) Indicate a signal transmission level was overrange (too high).

(4) Indicate that two consecutive digits/codes were received and stored in the other display memory (display without the blank).

4.104 Register (Address) Signaling Memory Storage

Note: Once a supervision module is enabled, the display and storage of register signaling cannot begin until a seizure condition is established in the enabled supervision module. When only register receivers are enabled, register information is displayed and stored in memory as soon as it is received.

4.105 Register signaling received at each input port (L1/L2) is stored in separate register data memories. The enabled register signaling receiver plug-in module(s) determines which input line (L1 or L2) is assigned to which data memory. Each data memory has 240 slots (individual memory locations) that can hold one register signaling digit or code.

4.106 The DISPLAY A memory shows a block of 16 slots on DISPLAY A while DISPLAY B shows the contents of 16 slots from the DISPLAY B memory. Each time a register signaling digit or code is observed, the appropriate display is immediately updated. Therefore, DISPLAYS A and B are real-time displays capable of presenting up to 240 register signaling digits/codes in groups of 16 digits/codes at a time.

4.107 In real-time operation, the position of a 16-digit/code group within a data memory is shown by the mainframe's LEAD DIGIT IDENT display. That is, the LEAD DIGIT IDENT display identifies the memory location of the digit/code currently showing in the left-most position of the A DISPLAY.

4.108 The sequential order in which register signaling digits/codes appear on DISPLAYS A and B depends on how the digits/codes are received and stored in the DISPLAY A and B memories. Figure 17 illustrates how a register signaling digit/code is assigned to a slot within an appropriate data memory. The rules used for storing digits/codes retain the exact order in which the digits/codes were received at the mainframe's two input ports (L1/L2).

4.109 Notice that two or more consecutive digits/codes stored in one data memory cause blank (space) slots in the other data memory. The blank slots appear in the appropriate DISPLAY (A or B) associated with the memory where stored.

4.110 The display memories stop accepting digits/codes once the 2760 enters a a latch state. Later, a reset signal normally releases the latch and clears DISPLAYS A and B. Storage of register signaling digits/codes can begin again starting from the first slot in the data memory. Thus, the data memories are effectively erased.

4.111 If the NO ERASE and the RESET AUTO switches are depressed, the reset signal from a plug-in module does not clear DISPLAYS A and B. The digits/codes from a new call are stored next to the digits/codes from the previous call. Two blanks (one blank on top of the other in the same slot position in each memory) separate the sets of digits/codes associated with the two calls. An operator manual or remote reset overrides the "no erase" condition.

Summarizing, blanks between register signals are used to:

(1) Separate sets of register signaling digits/codes from different calls. The NO ERASE and RESET AUTO switches must be depressed.

(2) Indicate a signal did not meet the minimum tone duration.

(3) Indicate that a received signal level was fully overrange.

(4) Indicate that two consecutive digits/codes were received and stored in the other display memory.

4.112 As previously mentioned:

(1) Each display shows a block of 16 slots from a data memory.

(2) A display is updated as soon as a register signaling digit/code is observed and decoded.

4.113 This means that when a digit/code is stored in any slot of an empty 16-slot block, that entire block is placed on the appropriate display. The displayed block fills up from left to right as more digits/codes arrive. The display continues to fill up until a digit/code is stored in the next 16-slot block. At this time, the new 16-slot block replaces the previously displayed block. This process continues until the 2760 enters a latch state or the entire 15-blocks (240 slots) of a data memory are used. A completely filled data memory causes the 2760 to enter a hard latch state. Because DISPLAYS A and B show entire blocks of 16-slots, the LEAD DIGIT IDENT also changes in increments of 16 (1, 17, 33, 49, 65 . . . etc.).

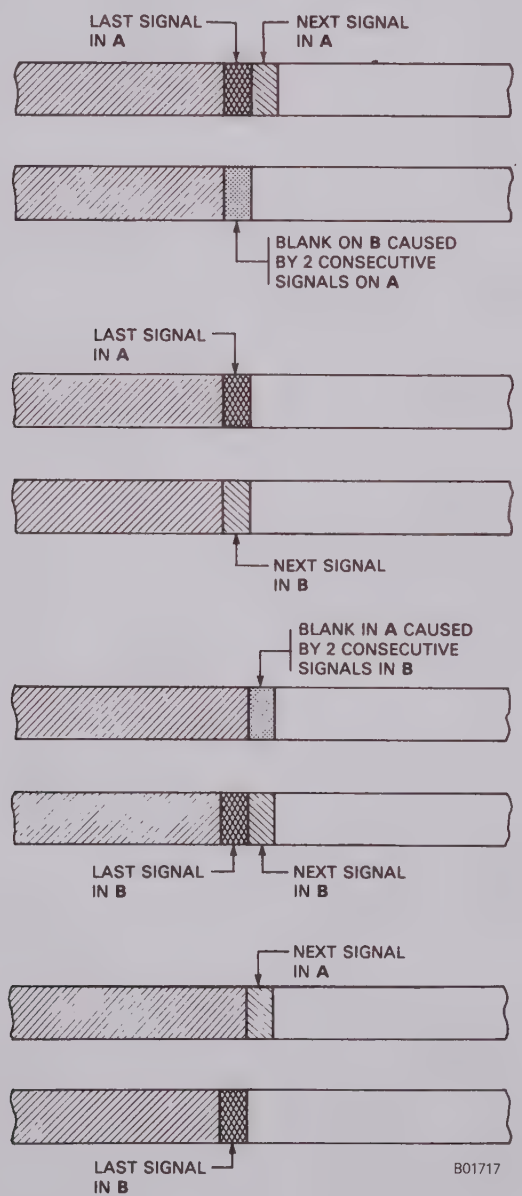

LAST SIGNAL IN A
NEXT SIGNAL IN A
BLANK ON B CAUSED BY 2 CONSECUTIVE SIGNALS ON A
LAST SIGNAL IN A
NEXT SIGNAL IN B
BLANK IN A CAUSED BY 2 CONSECUTIVE SIGNALS IN B
LAST SIGNAL IN B
NEXT SIGNAL IN B
NEXT SIGNAL IN A
LAST SIGNAL IN B
B01717

Fig. 17—Data Memory Storage Rules

Q. Plug-In Module Display Assignment

4.114 The Model 2760 is able to function simultaneously with two register (address) signaling modules and one line (supervision) signaling module. Each module must be assigned to either the A or B DISPLAY. Additional modules may be plugged into the 2760 mainframe assembly but only two register modules and one supervision module may be enabled at any one time.

4.115 Register and/or line signaling monitored information may be displayed in real time as received, and is also stored in memory for later review as desired. There are three separate memories. The three memories are:

- DISPLAY A Memory (240 slots)
- DISPLAY B Memory (240 slots)
- Supervision Memory (16 slots)

4.116 DISPLAYS A and B are normally used to show register signaling. Most associated supervision events are indicated by the six LEDs to the right of the displays. If desired, instead, supervision events may be shown on DISPLAY A with system clock time on DISPLAY B simply by depressing the RCL SUPV switch. Switching between register and line signaling displays may be done at any time, as often as desired during a call, without loss of data.

4.117 Obviously each plug-in module must be assigned to either the A or B DISPLAY. The plug-in module manuals provide instructions for display assignment.

4.118 The supervision module is always assigned to the A DISPLAY. Should two supervision modules be enabled at the same time, a display assignment conflict exists. The PGM ERR indicator will flash on and off to alert the operator.

4.119 If two register signaling plug-in modules are assigned to either the A or B DISPLAY a display assignment conflict again exists. The PGM ERR indicator will flash on and off to alert the operator.

4.120 The operator must resolve the conflict by eliminating the dual assignment. For some plug-in modules the EN indicator (on the module) will also flash on and off to identify the modules in conflict.

4.121 The operator resolves the display assignment conflict by disabling one of the two modules assigned to the same display. This is done by releasing the module's ENABLE switch.

R. Recall From Memory

4.122 The Model 2760 permits the recalling from memory of several various types of stored information. The dual display is used to show the recalled information. The three types of information that may be recalled are:

(1) Line (supervision) signaling

(2) Register (address) signaling

(3) Contents of comparison memory files.

4.123 Supervision

4.124 Line (supervision) signaling information for a call is recalled simply by depressing the RCL SUPV switch. Stored supervision information will appear on DISPLAY A and system clock time on DISPLAY B.

4.125 Register (Address) Signaling

4.126 The contents of the data memories may be reviewed at any time. Momentarily depressing either or both of the scroll/cursor (→ or ←)) control switches places the 2760 into a hard latch state and activates the cursor.

4.127 Entering a hard latch state (using a scroll/cursor control or the keypad) does not cause the immediate loss of register signaling data or line signaling (supervision) data. The contents of the display and supervision memories are held frozen until cleared by a manual reset, a remote reset, or a power-up reset. Therefore, an operator can review (using the scroll/cursor controls) the register signaling without losing the stored line signaling.

4.128 The cursor appears as a blinking of a pair of digits and/or codes on DISPLAYS A and B. Coincident with the blinking cursor, the enabled register receiver module(s) may also have lighted indicators. The lighted indicators describe component frequencies, delay, and overrange conditions for the blinking pair of digits and/or codes or blanks on the displays.

4.129 Horizontal Scroll

4.130 Momentarily depressing a scroll/cursor control moves the cursor over to the next position. See Fig. 18. Holding a scroll/cursor control depressed moves the cursor continuously at a 4-Hz rate. When the cursor reaches either end of the displays, other slots in the data memories are brought up and scrolled across the displays. Therefore, during data recall, displays act like 16-slot wide windows which can be placed anywhere across the data memories. The two windows move in unison.

4.131 Data recall can continue until the 1st or 240th slot has been displayed. The LED DIGIT IDENT display identifies the cursor position within the data memories. The A and B slots have a one-to-one correspondence during data reviewing. That is, if slot 8 from the A data memory appears in the extreme left-hand position of the A DISPLAY, then slot 8 of the B data memory also appears in the extreme left-hand position of DISPLAY B, etc.

4.132 Vertical Scroll

4.133 Momentarily depressing both scroll/cursor control switches at the same time moves the cursor in increments of 16 slots. The display shows new data in blocks of 16 slots each time. Holding both scroll/cursor control switches depressed moves the cursor in increments of 16 slots continuously at a rate of 4-Hz. Figure 18 shows a conceptual drawing of the vertical scroll for one display.

4.134 Recall that DISPLAYS A and B show data in unison. When each block in corresponding pairs of blocks about to be shown does not contain data then the cursor jumps back to slot 1. Thus, only pairs of blocks with data (in either block) appear on the displays . . . pairs of blocks void of data are not displayable in the vertical scroll mode.

4.135 Comparison Memory Files

4.136 The contents of comparison memory files may be recalled using the procedures described in Part H. Comparison Memory Programming.

S. Country and City Codes

4.137 By international agreement the world has been divided into nine World Zones. In addition each country and major city has been assigned a special code. This enables the assignment of a unique telephone number to each subscriber in the world.

4.138 Table S shows the present assigned country and city codes. The first digit of each country code is the World Zone the country is located in. Country codes may consist of one, two, or three digits.

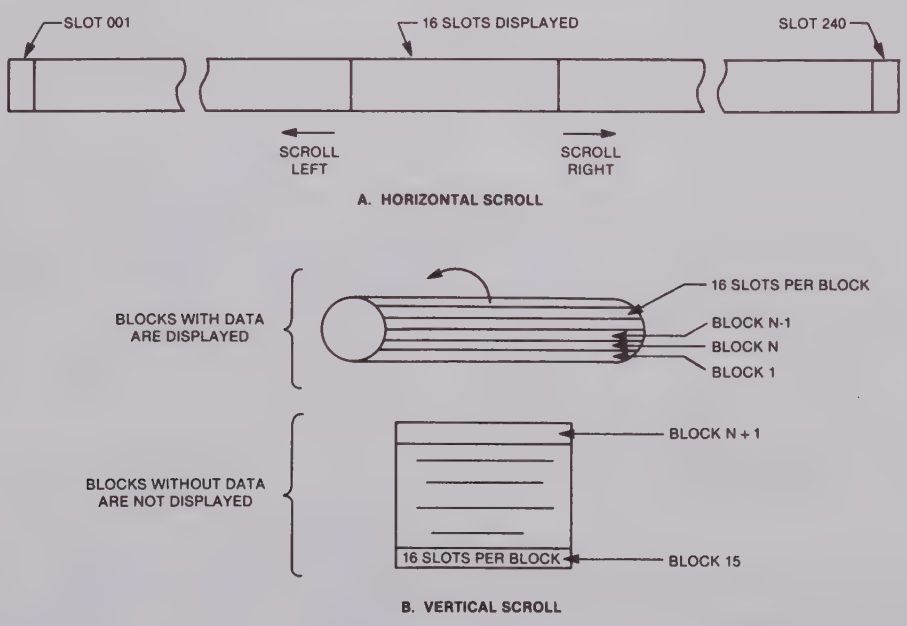


Fig. 18—Display Scroll Formats

TABLE S

Dial Countries—Rates, Country, and City Codes

Effective October 2, 1983

During the holiday season, you'll find it easier to get through if you avoid calling on Christmas or New Year's Day. Instead, try your calls on the days before and after these holidays.

UNITED KINGDOM/IRELAND		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	6PM-7AM	1.25	5.70	10.10	.76
Discount	1PM-6PM	1.56	5.70	10.10	.95
Standard	7AM-1PM	2.08	5.70	10.10	1.26

Country Codes		City Codes	EST Time
Ireland	353	Cork 21, Dublin 1, Galway 91, Limerick 61, Waterford 51	5
United Kingdom	44	Belfast 232, Birmingham 21, Glasgow 41, London 1	5

EUROPE		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	6PM-7AM	1.42	7.05	12.60	.80
Discount	1PM-6PM	1.78	7.05	12.60	1.00
Standard	7AM-1PM	2.37	7.05	12.60	1.33

Country Codes		City Codes	EST Time
Andorra	33	All Points 078	6
Austria	43	Graz 316, Linz Donau 732, Vienna 222	6
Belgium	32	Antwerp 3, Brussels 2, Ghent 91, Liege 41	6
Cyprus	357	Limassol 51, Nicosia 21, Paphos 61	7
Czechoslovakia	42	Bratislava 7, Brno 5, Havirov 6994, Ostrava 69, Praha 2	6
Denmark	45	Aalborg 8, Aarhus 6, Copenhagen 1 or 2, Odense 9	6
Finland	358	Espoo Esbo 0, Helsinki 0, Tampere 31, Turku 21	7
France	33	Lyon 7, Marseille 91, Nice 93, Paris 1	6
German Dem. Rep.	37	Berlin 2, Dresden 51, Leipzig 41, Magdeburg 91	6
Germany, Fed. Rep. of	49	Berlin 30, Bonn 228, Hamburg 40, Munich 89	6
Greece	30	Athens 1, Iraklion, Crete 81, Larissa 41, Piraeus 1	7
Hungary	36	Budapest 1, Derbrecen 52, Gyor 96, Miskolc 46	6
Iceland	354	Akureyri 6, Hafnarfjorour 1, Reykjavik 1	5
Italy	39	Florence 55, Genoa 10, Milan 2, Naples 81, Rome 6	6
Liechtenstein	41	All Points 75	6
Luxembourg	352	*	6
Monaco	33	All Points 93	6
Netherlands	31	Amsterdam 20, Rotterdam 10, The Hague 70	6
Norway	47	Bergen 5, Oslo 2, Stavanger 4, Trondheim 75	6
Poland	48	Warsaw 22	6
Portugal	351	Coimbra 39, Lisbon 1, Porto 2, Setubal 65	5
Romania	40	Bucuresti 0, Cluj-Napoca 51, Constanta 16	7
San Marino	39	All Points 541	6
Spain	34	Barcelona 3, Madrid 1, Seville 54, Valencia 6	6
Sweden	46	Goteborg 31, Malmo 40, Stockholm 8, Vasteras 21	6
Switzerland	41	Basel 61, Berne 31, Geneva 22, Zurich 1	6
Turkey	90	Adana 711, Ankara 41, Istanbul 11, Izmir 51	8
Vatican City	39	All Points 6	6
Yugoslavia	38	Belgrade 11, Sarajevo 71, Skoplje 91, Zagreb 41	6

CENTRAL AMERICA		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	11PM-8AM	1.57	6.30	9.45	.68
Discount	8AM-5PM	1.97	6.30	9.45	.85
Standard	5PM-11PM	2.62	6.30	9.45	1.13

Country Codes		City Codes	EST Time
Belize	501	Belize City,* Corozal Town 04, Punta Gorda 07	−1
Costa Rica	506	*	−1
El Salvador	503	*	−1
Guatemala	502	Antigua,* Guatemala City 2, Quezaltenango*	−1
Honduras	504	*	−1
Nicaragua	505	Chinandega 341, Diriamba 42, Leon 31, Managua 2	−1
Panama	507	*	0

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TABLE S (Cont)

Dial 011 or 01 + Country Code + City Code + Local Number

AFRICA		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	5PM-6AM	1.73	9.45	12.60	.89
Discount	12 Noon-5PM	2.17	9.45	12.60	1.11
Standard	6AM-12 Noon	2.89	9.45	12.60	1.48

Country Codes		City Codes	EST Time
Algeria	213	*	6
Cameroon	237	*	6
Egypt	20	Alexandria 3, Aswan 97, Asyout 88, Benha 13, Cairo 2	7
Ethiopia	251	Addis Ababa 1, Akaki 1, Asmara 4, Assab 3, Awassa 6	8
Gabon	241	*	6
Ivory Coast	225	*	5
Kenya	254	Kisumu 35, Mombasa 11, Nairobi 2, Nakuru 37	8
Liberia	231	*	5
Libya	218	Benghazi 61, Misuratha 51, Tripoli 21, Zawia 23	6
Malawi	265	Balaka,* Blantyre,* Bvumbwe,* Chileka,* Dedza*	7
Morocco	212	Agadir 8, Beni-Mellal 48, Casablanca,* El Jadida 34	5
Namibia	264	Grootfontein 673, Keetmanshoop 631, Mariental 661	7
Nigeria	234	Lagos 1	6
Senegal	221	*	5
South Africa	27	Cape Town 21, Durban 31, Johannesburg 11	7
Tunisia	216	Bizerte 2, Kairouan 7, Msel Bourguiba 2, Tunis 1	6

PACIFIC		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	11PM-10AM	2.53	9.45	12.60	.95
Discount	10AM-5PM	3.17	9.45	12.60	1.19
Standard	5PM-11PM	4.22	9.45	12.60	1.58

Country Codes		City Codes	EST Time
American Samoa	684	*	−6
Australia	61	Adelaide 8, Brisbane 7, Melbourne 3, Sydney 2	15
Fiji	679	*	17
French Polynesia	689	*	−5
Guam	671	*	15
Hong Kong	852	Hong Kong 5, Kowloon 3, Sha Tin 0	13
Indonesia	62	Jakarta 21, Medan 61, Semarang 24	12
Korea, Rep. of	82	Incheon 32, Pusan 51, Seoul 2, Taegu 53	14
Malaysia	60	Ipoh 5, Johor Bahru 73, Kelang 3, Kuala Lumpur 3	13
New Caledonia	687	*	16
New Zealand	64	Auckland 9, Christchurch 3, Dunedin 24, Hamilton 71	17
Papua New Guinea	675	*	15
Phillippines	63	Cebu 32, Davao 35, Iloilo 33, Manila 2	13
Saipan	670	*	15
Singapore	65	*	13
Taiwan	886	Kaohsiung 7, Tainan 62, Taipei 2	13
Thailand	66	Bangkok 2	12

INDIAN OCEAN		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	11AM-6PM	3.13	12.60	14.20	1.30
Discount	1AM-11AM	3.92	12.60	14.20	1.63
Standard	6PM-1AM	5.22	12.60	14.20	2.17

Country Codes		City Codes	EST Time
Pakistan	92	Abbotabad 5921, Bahawalpur 621, Faisalabad 411	10
Sri Lanka	94	Colombo 1, Kandy 8, Moratuwa 72	10½

Time Differences: The time column is used to calculate the time in the country you are calling. If you live in the Eastern Standard Time zone, add the hours opposite the country you are calling to your local standard time (subtract if preceded by a minus sign). For Central add 1 hour, Mountain add 2 hours and Pacific add 3 hours to the time column number and then add that number to your local standard time. Countries with more than one time zone are based upon the following cities: Sydney, Australia, Rio de Janeiro, Brazil, Tahiti, French Polynesia, Jakarta, Indonesia, and Kuala Lumpur, Malaysia.

TABLE S (Cont)

SOUTH AMERICA		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	10PM-7AM	1.66	9.45	12.60	.71
Discount	1PM-10PM	2.08	9.45	12.60	.89
Standard	7AM-1PM	2.77	9.45	12.60	1.18

Country Codes		City Codes	EST Time
Argentina	54	Buenos Aires 1, Cordoba 51, La Plata 21, Rosario 41	2
Bolivia	591	Cochabamba 42, La Paz 2, Santa Cruz 33	1
Brazil	55	Belo Horizonte 31, Rio de Janeiro 21, Sao Paulo 11	2
Chile	56	Concepcion 42, Santiago 2, Valparaiso 31	1
Colombia	57	Barranquilla 5, Bogota,* Cali 3, Medellin 4	0
Ecuador	593	Ambato 2, Cuenca 4, Guayaquil 4, Quito 2	0
Guyana	592	Bartica 5, Georgetown 2, New Amsterdam 3	2
Paraguay	595	Asuncion 21, Concepcion 31	1
Peru	51	Arequipa 54, Callao 14, Lima 14, Trujillo 44	0
Suriname	597	*	1½
Uruguay	598	Canelones 332, Mercedes 532, Montevideo 2	2
Venezuela	58	Barquisimeto 51, Caracas 2, Maracaibo 61, Valencia 41	1

NEAR EAST		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	3PM-9PM	2.21	9.45	12.60	.80
Discount	9PM-8AM	2.76	9.45	12.60	1.00
Standard	8AM-3PM	3.68	9.45	12.60	1.33

Country Codes		City Codes	EST Time
Bahrain	973	*	8
Iran	98	Isfahan 31, Mashad 51, Tabriz 41, Teheran 21	8½
Iraq	964	Baghdad 1, Basra 40, Hilla 30, Mousul 60	8
Israel	972	Haifa 4, Jerusalem 2, Ramat Gan 3, Tel Aviv 3	7
Jordan	962	Amman 6, Irbib 2, Jerash 4, Karak 3, Ma'am 3, Ramtha 2	7
Kuwait	965	*	8
Oman	968	*	9
Qatar	974	*	8
Saudi Arabia	966	Hofuf 3, Jeddah 2, Makkah (Mecca) 2, Riyadh 1	8
United Arab Emirates	971	Abu Dhabi 2, Ajman 6, Al Ain 3, Dubai 4, Sharjah 6	9
Yemen Arab Republic	967	Amran 2, Sana 2, Taiz 4, Yarim 4, Zabid 3	8

CARIBBEAN/ATLANTIC		Initial Period Rate			Additional Minute Rate
		1 Minute	3 Minute	3 Minute	
Rate Levels	Hours	Dial	Station	Person	All Calls
Economy	10PM-7AM	1.01	6.30	9.45	.68
Discount	7AM-4PM	1.26	6.30	9.45	.85
Standard	4PM-10PM	1.68	6.30	9.45	1.13

Country Codes		City Codes	EST Time
French Antilles	596	*	1
Guantanamo Bay (U.S. Naval Base)	53	All points 99	0
Haiti	509	Cap Hatien 3, Gonaive 2, Port Au Prince 1	0
Netherlands Antilles	599	Aruba 8, Bonaire 7, Curacao 9, St. Maarten 5	1

*City Code(s) Not Required.

To call points listed below, dial 1 + 809 + Local Number.

Anguilla	Bermuda	Jamaica	St. Kitts
Antigua	British Virgin Islands	Montserrat	St. Lucia
Bahamas	Cayman Islands	Mustique	St. Vincent
Barbados	Dominica	Nevis	Trinidad and Tobago
Bequia	Dominican Republic	Palm Island	Union Island

Rate is determined by the time of day at the originating telephone.

Rates are in effect seven days a week.

Calls requiring special operator assistance (person, collect, calling card, time and charges, etc.) are charged at higher rates. Rates apply only for countries listed. For rates to other countries and complete rate information call toll-free **1 800 874-4000.**

Calls Originating Overseas. Collect calls are billed at the Person rate only. Additional minutes for collect and calling card calls are billed at Standard and Discount rates only.

Federal excise tax of 3% is added on all calls billed in the U.S.

5.18 The 1 kHz signal enables the display clock which uses the RAM data to automatically refresh display board digits and LEDs.

5.19 Display Board A4

5.20 Refer to Fig. 19. The A4 Display Board is provided with thirty-six 7-segment digit displays, ten LEDs, and eight switches. These components are grouped into three major circuits:

(1) Dual 16-digit display

(2) 3-digit and 10-LED display

(3) 8-switch pushbutton control.

5.21 The 7-segment indicators are arranged into the two 16-digit groups designated display A and display B. The Display Driver Board supplies segment information to display A on one set of eight lines, and segment information to display B on another set of eight input lines; however, both display groups are supplied with a common set of sixteen driver lines. These anode lines are multiplexed so that each indicator anode is turned on for 1 msec and turned off for 21 msec.

5.22 Only three of the four LEDs provided the LDI (LEAD DIGIT IDENTIFIER) are used for display, and lead zero blanking is not done. The LDI display is supplied by dedicated segment lines and anode drive lines. The LDI segment lines are shared with the ten LED indicators which provide system status and supervision indications. These status and supervision LEDs are driven with two separate cathode driver lines.

5.23 Each of the eight, normally opened, pushbutton switches are tied to +5 V through pull-up resistors. When depressed, each switch presents a ground signal for the Data Bus.

E. System Controller Section

5.24 Refer to Fig. 20. The system controller comprises the 8080 Processor Board A8, Interface Board A6, 4K RAM Board A9, ROM/RAM Board A10, and additional memory addressed 1/0 locations within the mainframe as well as utilized plug-in modules.

5.25 Processor Board A8

5.26 Refer to Fig. 19. The 8080 Processor Board provides the intelligence required to process input data for an orderly and correct storage and display of information.

5.27 An Intel 8080 CPU, clock generator, and system controller together with read/write, timing, and interface controls comprise the processor circuitry.

5.28 The Processor Board uses 3-bus architecture – Data, Address, and Control Buses – to interface a "Memory Mapped 1/0" scheme which allows a single array of both memory data and 1/0 addressed functions. Also, the processor is interrupt driven and processes service request on an established priority basis.

5.29 Shortly after mainframe power-up, the processor is reset to restore internal programming to initial condition. Program executions begin with an initialization program, and then the mainframe's stored background routine is effected. Mainframe pushbutton provisions also allow automatic or manual reset of processor programming.

5.30 System/Processor Data Bus gating is effected with Address and Control Bus signaling.

5.31 Interface Board A6

5.32 Refer to Fig. 19. The Interface Board functions to interface active memory mapped plug-in modules to the mainframe's 8080 processor controlled memory storage and display assembly.

5.33 The Interface Board consists of the following functional circuits.

(1) An assignment detector circuit ensures each individual monitor operation is assigned to only one plug-in module.

(2) The priority encoder accepts up to eight plug-in interrupt requests, determines the highest priority, compares each request against a software controlled current status register, and issues interrupt commands to the 8080 Processor Board.

(3) The timer interrupt circuit interrupts the 8080 processor at specific intervals to update system timing.

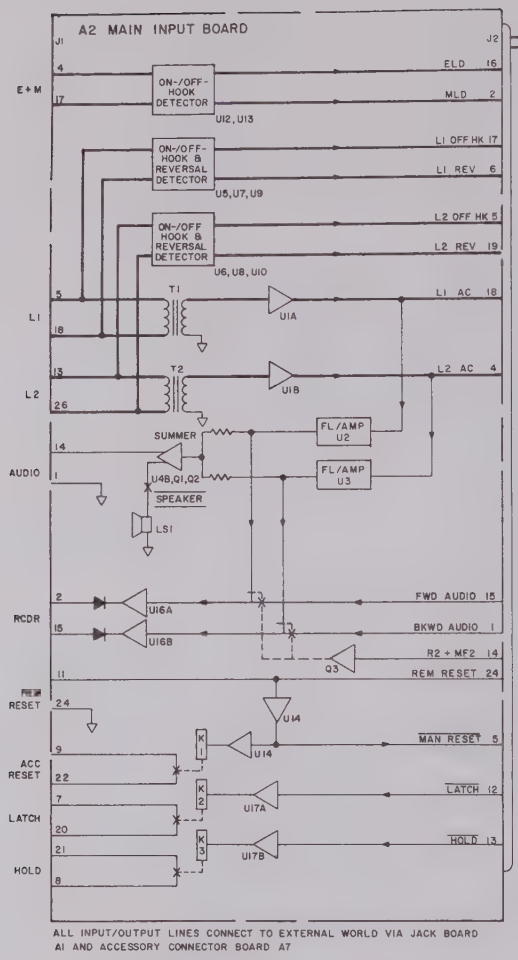
(4) The processor controlled timer establishes timing throughout the Model 2760 system.

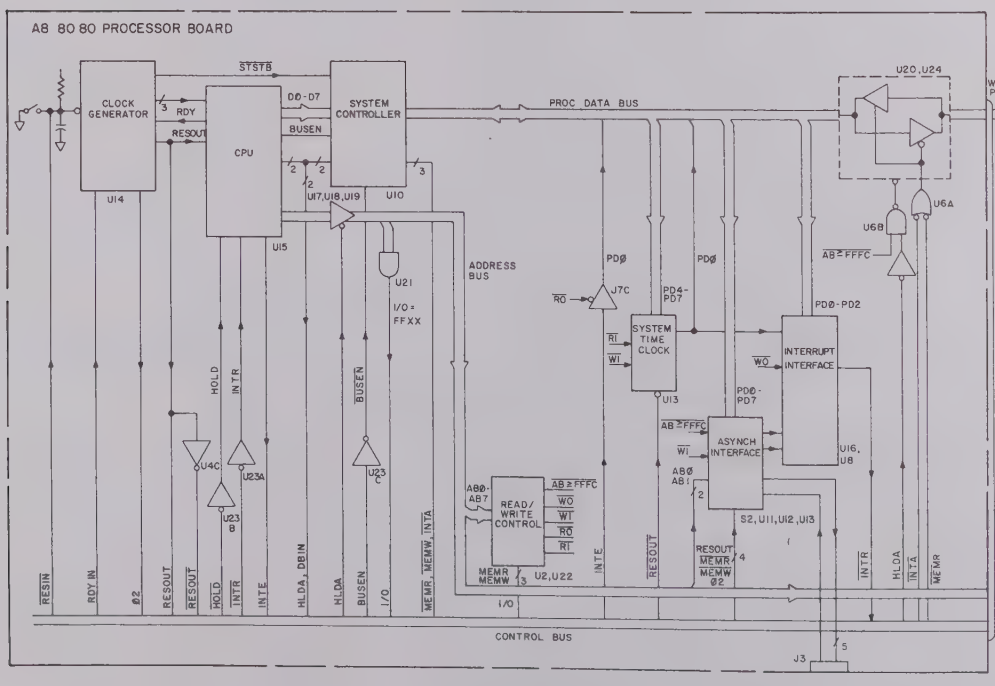
(5) Flip-flop circuits process the manual reset command and generate latch and hold commands.

(6) Read/write and address decoding for various memory mapped system functions.

5.34 Memory Boards A9 and A10

5.35 RAM Board A9 provides 4K of memory for both mainframe and plug-in module software, and ROM/RAM Board A10 provides 7K of ROM and 1K of RAM memory for mainframe programming software.


A2 MAIN INPUT BOARD
J1
J2
E+M
ON-/OFF-HOOK DETECTOR
U12, U13
ELD 16
MLD 2
ON-/OFF-HOOK & REVERSAL DETECTOR
U5, U7, U9
LI OFF HK 17
LI REV 6
ON-/OFF HOOK & REVERSAL DETECTOR
U6, U8, U10
L2 OFF HK 5
L2 REV 19
L1
T1
U1A
LI AC 18
L2
T2
U1B
L2 AC 4
SUMMER
FL/AMP U2
FL/AMP U3
AUDIO
U4B, Q1, Q2
SPEAKER
LS1
RCDR
U16A
U16B
FWD AUDIO 15
BKWD AUDIO 1
R2 + MF2 14
Q3
REM RESET 24
RESET
U14
MAN RESET 5
ACC RESET
LATCH
U17A
LATCH 12
HOLD
U17B
HOLD 13
ALL INPUT/OUTPUT LINES CONNECT TO EXTERNAL WORLD VIA JACK BOARD
AI AND ACCESSORY CONNECTOR BOARD A7


A8 8080 PROCESSOR BOARD
CLOCK GENERATOR
U14
STSTB
RDY
RESOUT
CPU
U15
D0-D7
BUSEN
SYSTEM CONTROLLER
U10
U17, U18, U19
PROC DATA BUS
U20, U24
U6A
U6B
AB ≥ FFFC
ADDRESS BUS
U21
I/O = FFXX
RD
J7C
PD0
PD4-PD7
SYSTEM TIME CLOCK
U13
RI
WI
WO
INTERRUPT INTERFACE
PD0-PD2
PD0-PD7
ASYNCH INTERFACE
U16, U8
AB0 AB1
S2, U11, U12, U13
HOLD
INTR
BUSEN
U4C
U23A
U23B
U23
AB0-AB7
READ/WRITE CONTROL
RO
MEMR
MEMW
U2, U22
INTE
RESOUT
MEMR
MEMW
Ø2
I/O
HLDA
INTA
RESIN
RDY IN
HLDA, DBIN
MEMR, MEMW, INTA
CONTROL BUS
J3
W5P4
W3P3
W5P1
DB0-DB7
AB0-AB15
FFCIR
A6 INT
RESIN, R

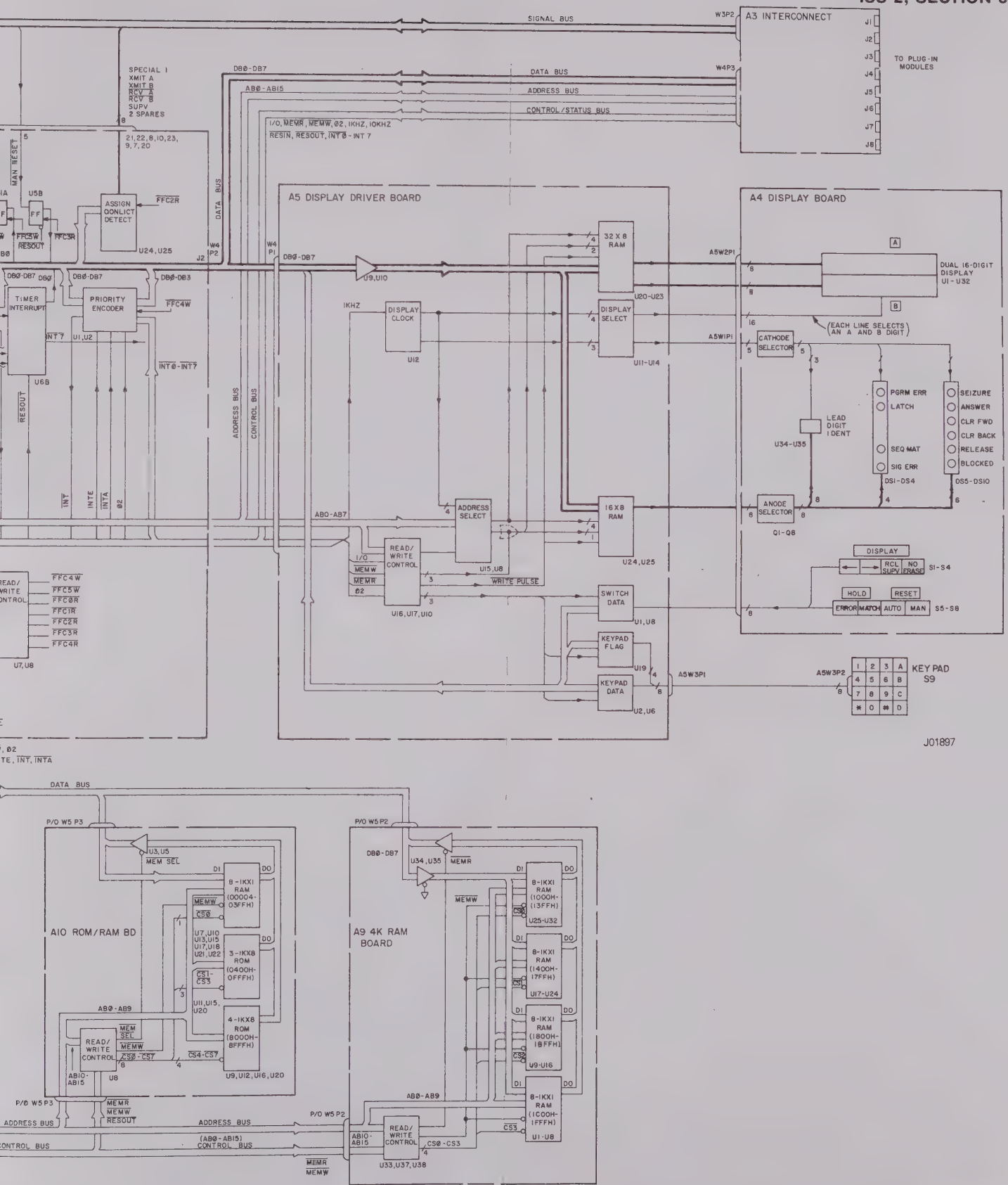


Fig. 19—Model 2760 Mainframe Functional Diagram

6. MAINTENANCE

A. General

6.01 This part contains maintenance and alignment information for the mainframe assembly of the Model 2760 Universal Signaling Analyzer.

6.02 With the exception of the one "resident module" housed in the mainframe assembly, this part does not contain maintenance and alignment information for the various receiver plug-in modules (R2/MFC, MF2, MF3, E&M, etc.) associated with the Model 2760 Analyzer.

B. Service Information

6.03 Complete warranty information is contained in the purchase order agreement under terms and conditions of sale. Summarized briefly, the Northeast Electronics warranty extends for a period of one year to the original purchaser of a test instrument.

6.04 It is recommended that Northeast Electronics' Repair Department be contacted for assistance if, for any reason, a Northeast product fails to perform as expected. This step eliminates the needless delay entailed when a product is returned unnecessarily. Contact the Repair Department at Northeast Electronics, P.O. Box 2021, Concord, New Hampshire 03301, telephone: (603) 228-3700.

6.05 If a Northeast Electronics product requires factory servicing during the warranty period, be sure to include a ship-to address and a description of the problem when returning the product to Northeast Electronics. After the warranty period has expired, equipment returned must be accompanied by all of the following:

- The number of the purchase order covering the cost of servicing
- Bill-to address
- Ship-to address
- Description of problem.

6.06 In all cases, equipment requiring factory servicing should be sent to the Repair Department at the preceding address and telephone number. A return material authorization (RMA) number is not required, but will be provided by the Repair Department upon request.

C. Fan Motor Servicing

6.07 The mainframe houses a cooling fan unit that may require periodic inspection and cleaning. The fan unit is internally located at the right side when facing the mainframe's rear side.

6.08 To gain access to the fan unit, perform the following steps:

(1) Set the POWER switch to OFF and disconnect the mainframe's power cord.

(2) Remove the mainframe's bottom cover.

(3) Carefully allow the fan unit to drop out of the mainframe assembly by removing the five mounting screws which secure the fan in place.

Note: In addition to inspection and cleaning of the fan motor, also remove any obstruction from the air flow ports located in the mainframe's rear wall.

(4) To replace the fan, ensure that all interior ribbon cables are clear of the fan unit and reverse the order and procedures of steps 1 through 4.

D. DC Voltage Checks

6.09 The +5 Vdc and ±12 Vdc power supply units are factory calibrated for correct mainframe operations. The +5 Vdc and ±12 Vdc adjustment procedures presented in paragraphs 6.10 and 6.11 are necessary only if power supply outputs fail to comply with the following voltage checkout procedure:

(1) Obtain a dc voltmeter with a ± 0.1% accuracy (Simpson #464, or equivalent).

(2) Place the mainframe's POWER switch to OFF.

(3) Remove the mainframe's top cover to expose Processor Board (A8).

(4) Locate the black, white, red, and violet wired standoffs which are found near the left end of the ribbon cable connection on the processor board.

(5) Connect the black wired standoff as a common ground for the dc voltmeter.

(6) Place the POWER switch ON, and check for the following voltage levels:

DC VOLTAGE	AT	POINT
+5.15 ± 0.05 Vdc	Red wired standoff
+12.00 ± 0.1 Vdc	White wired standoff
−12.00 ± 0.1 Vdc	Violet wired standoff

(7) Refer to the appropriate +5 Vdc and/or ±12 Vdc adjustment procedure(s) if the above voltage level requirements are not met. If the voltage checks are "good", place the POWER switch to OFF and reassemble the mainframe.

E. +5 Vdc (PS1) Adjustment Procedure

6.10 PREPARATION FOR ADJUSTMENT
(Refer to Fig. 21.)

(1) Obtain a dc voltmeter with a ±0.1% accuracy and prepare a resistive load network equivalent to 0.7 ohms, 40 watts.

(2) Place the mainframe POWER switch to OFF and remove the top cover of the mainframe.

(3) Raise the ribbon cable which rests against the −5 Vdc housing to expose the OVP (Over-Voltage Protection) adjustment port.

(4) Remove the four screws which hold the 4K RAM Board (A9), and displace the board as necessary to gain easy access to the OVP adjustment port.

(5) Disconnect the two 2-pin connectors located just in front of the OVP port.

(6) Remove the top cover of the −5 Vdc housing assembly.

(7) Remove all four leads at the S ± output terminals and connect the 0.7 ohm, 40 watt resistive load network across the S± terminals. Also, connect the dc voltmeter to S+ (positive lead) and to S− (common lead).

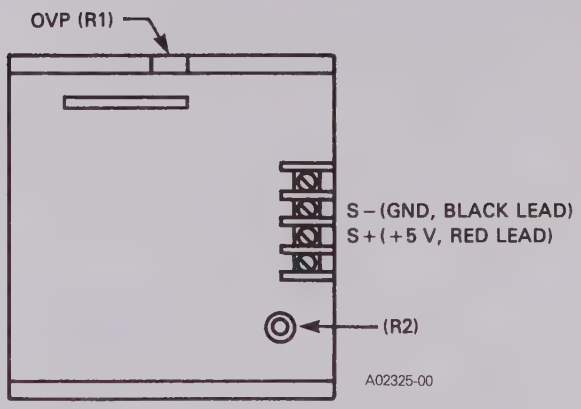


Fig. 21—+5 Vdc Power Supply (PS1)

6.11 +5 VOLT ADJUSTMENT
(Refer to Fig. 21.)

(1) Set the OVP (R1) adjust to the full clockwise position.

(2) Place the mainframe POWER switch to ON.

(3) Set the +5 volt (R2) adjust for a voltmeter reading of 6.0 ± 0.5 volts.

(4) Adjust OVP (R1) slowly counterclockwise and stop when the dc voltmeter reads between 0.0 volts and 1.0 volts.

(5) Set the POWER switch to OFF.

(6) Set R2 fully counterclockwise.

(7) Place the POWER switch to ON.

(8) While observing the dc voltmeter for a reading of +6.0 ± 0.2 volts, adjust R2 slowly clockwise until the voltage drops to a reading between 0.0 volts and +1.0 volts. If the first reading of the dc voltmeter was not between 5.80 Vdc and 6.2 Vdc, repeat steps 1 thru 8.

(9) Place the POWER switch to OFF.

(10) Turn the +5 volt (R2) adjust to the full counterclockwise position.

(11) Place the POWER switch to ON.

(12) Adjust R2 for a voltmeter reading of 5.25 ± 0.01 volts.

(13) Place the POWER switch to OFF.

(14) Disconnect the dc voltmeter and the resistive load network from the +5 volts (S±) output terminals, and re-connect the output leads to S+ (red) and S− (black).

(15) Replace the 4K RAM board.

(16) Connect the dc voltmeter across the +5 input (red and black wired standoffs) on Processor Board (A8).

(17) Place POWER switch to ON.

(18) Observe a voltmeter reading of +5.15 ± 0.05. Repeat steps 9 thru 18 if the reading is not between +5.10 volts and +5.20 volts.

(19) Place the POWER switch to OFF.

(20) Disconnect the dc voltmeter from Processor Board (A8).

(21) Re-connect the two 2-pin slip connectors located just in front of the +5 volt OVP adjustment port, and reposition the ribbon cable over the OVP.

(22) Replace the top cover of the +5 Vdc housing assembly and install the 4K RAM Board.

F. ±12 Vdc (PS2) Adjustment Procedure

6.12 PREPARATION FOR ADJUSTMENT
(Refer to Fig. 22.)

(1) Obtain a dc voltmeter with a ±0.1% accuracy, and prepare two resistive load networks equivalent to 12 ohms, 12 watts.

(2) Set the mainframe's POWER switch to OFF, remove the top cover of the +5 V supply, and remove the four screws which mount the supply in place.

(3) Displace the +5 Vdc power supply as required to allow access to the ±12 Vdc power supply, and disconnect the ±12 volt supply's 4-pin, mate'n lock connector.

(4) Pull out and displace the resident module away from the mainframe.

(5) Remove dress panels (and/or plug-in modules) as required to gain access to the four screws which mount the ±12 volt power supply.

(6) Remove the four mounting screws and carefully remove the ±12 volt power supply by way of the removed resident module.

(7) Disconnect the output leads (white, black, and violet) of the power supply. Connect a 12 ohm, 12 watt resistive network across the +12 volt output, and connect a 12 ohm, 12 watt resistive network across the −12 volt output.

(8) Remount the +5 volt supply in place and replace the supply's top cover.

(9) Set the ±12 volt supply on top of the +5 volt housing unit, and re-connect the ±12 volt supply's 4-pin, mate'n lock connector.

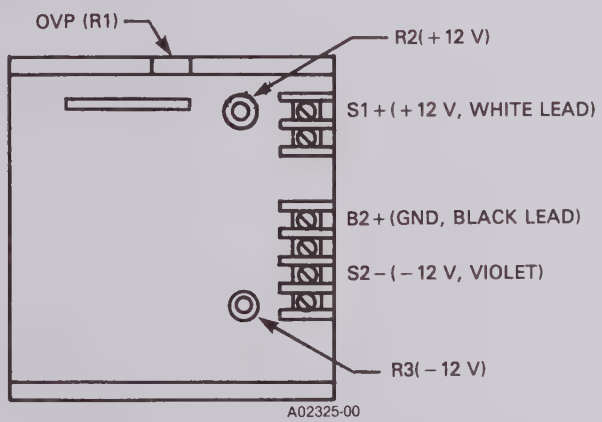


Fig. 22—±12 Vdc Power Supply (PS2)

6.13 ±12 VOLT ADJUSTMENT
(Refer to Fig. 22.)

(1) Turn the ±12 volt supply's OVP (R1) adjust fully clockwise.

(2) Connect the dc voltmeter directly across the +12 volt (red lead) and −12 volt (blue lead) terminals.

(3) Place the mainframe's POWER switch to on.

(4) Set the +12 volt (R2) adjust for a dc voltmeter reading of 26.50 ± 0.1 volts.

(6) Place the POWER switch to OFF.

(7) Turn R2 fully counterclockwise.

(8) Place the POWER switch to ON.

(9) While observing the voltmeter for a reading between 26.30 volts and 26.70 volts, adjust R2 slowly clockwise until the reading drops to a reading between 0.0 volts and 1.0 volts. If the last reading before switching was not between 26.30 volts and 26.70 volts repeat steps 1 thru 9.

(10) Place the POWER switch to OFF.

(11) Turn R2 fully counterclockwise.

(12) Connect the dc voltmeter across the +12 volt (white lead) and the ground (black lead) output terminals of the supply.

(13) Place the POWER switch to ON.

(14) Adjust R2 for a voltmeter reading of +12.00 ± 0.10 volts.

(15) Connect the voltmeter across the −12 volt (violet lead) and the ground (black lead) output terminals of the supply.

(16) Set the −12 volt (R3) adjust for a voltmeter reading of −12.00 ± 0.10 volts.

(17) Place the POWER switch to OFF.

(18) Disconnect the dc voltmeter, the resistive load, and the supply's 4-pin mate'n lock connector. Connect the output leads (white, black, and violet of the ±12 volt supply, then use the empty resident module entrance to return the ±12 volt supply to its proper position within the mainframe, and re-connect the supply's 4-pin mate'n lock connector. Dislodge the +5 volt supply as necessary to ensure proper installation of the ±12 volt supply.

G. Main Input Board Adjustment

(1) Place the POWER switch to OFF.

(2) Remove the screws which secure the resident module to the mainframe. Pull out the resident module as necessary to expose adjustment potentiometers R37, R38, R43, and R44.

(3) Use the standoff located between potentiometers R37 and R38 as a convenient ground reference for the dc voltmeter and adjust the potentiometers as follows:

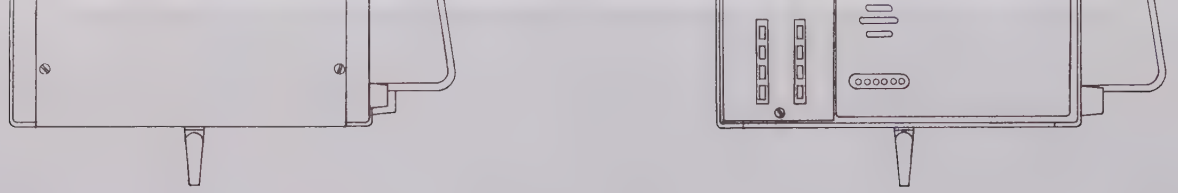
POT	DC VOLTAGE AT	POINT
R37	−2.5 ± 0.2	U5-3
R38	−2.5 ± 0.2	U6-3
R43	+6.0 ± 0.2	U7-3
R44	+6.0 ± 0.2	U8-3

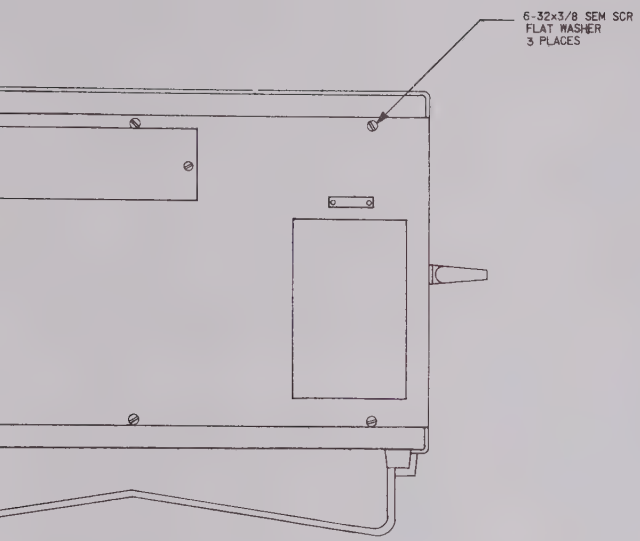
(4) Disconnect the dc voltmeter and replace the resident module into the mainframe.

7. DIAGRAMS

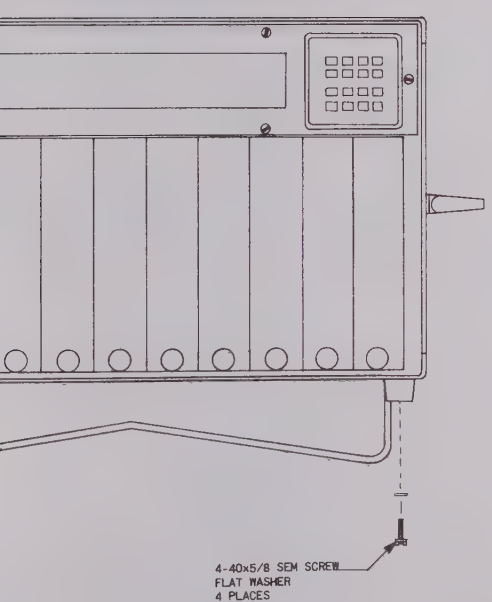
A. General

7.01 This part contains a functional diagram, parts location diagrams, and schematic diagrams for the Model 2760 Universal Signaling Analyzer mainframe.

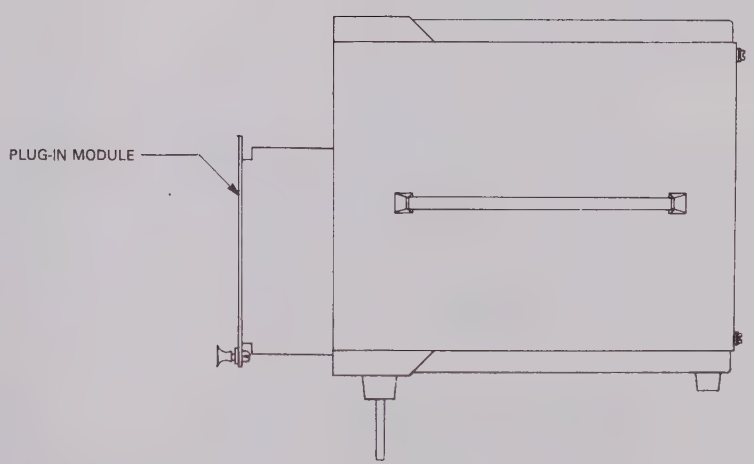




BACK VIEW



FRONT VIEW

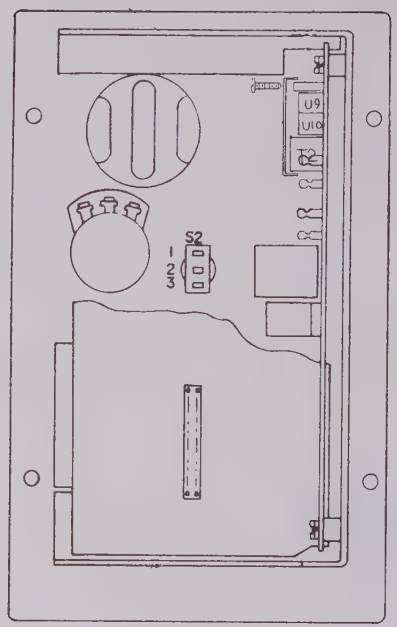


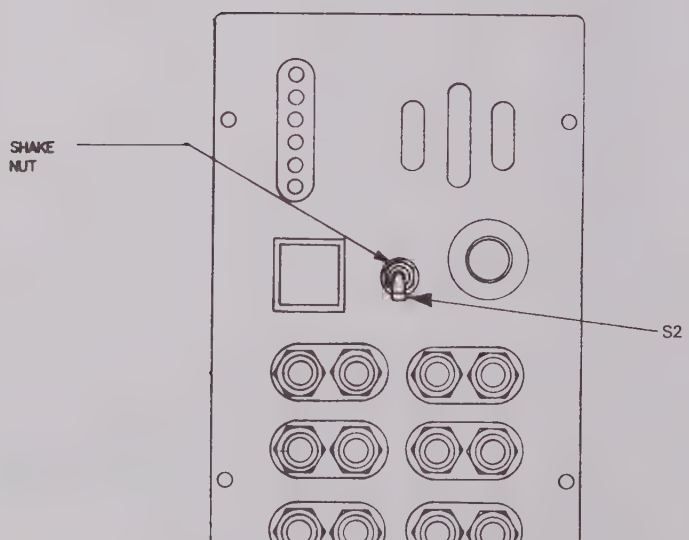
SIDE VIEW

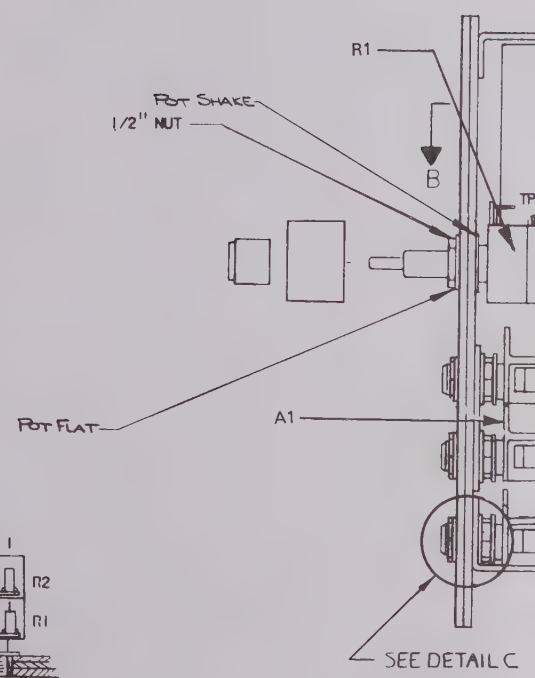
Ref. E2760-00-900-9

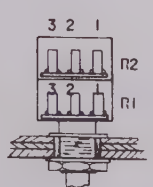
Fig. 23—Model 2760 Mainframe Assembly Diagram

VIEW A-A









SECTION B-B

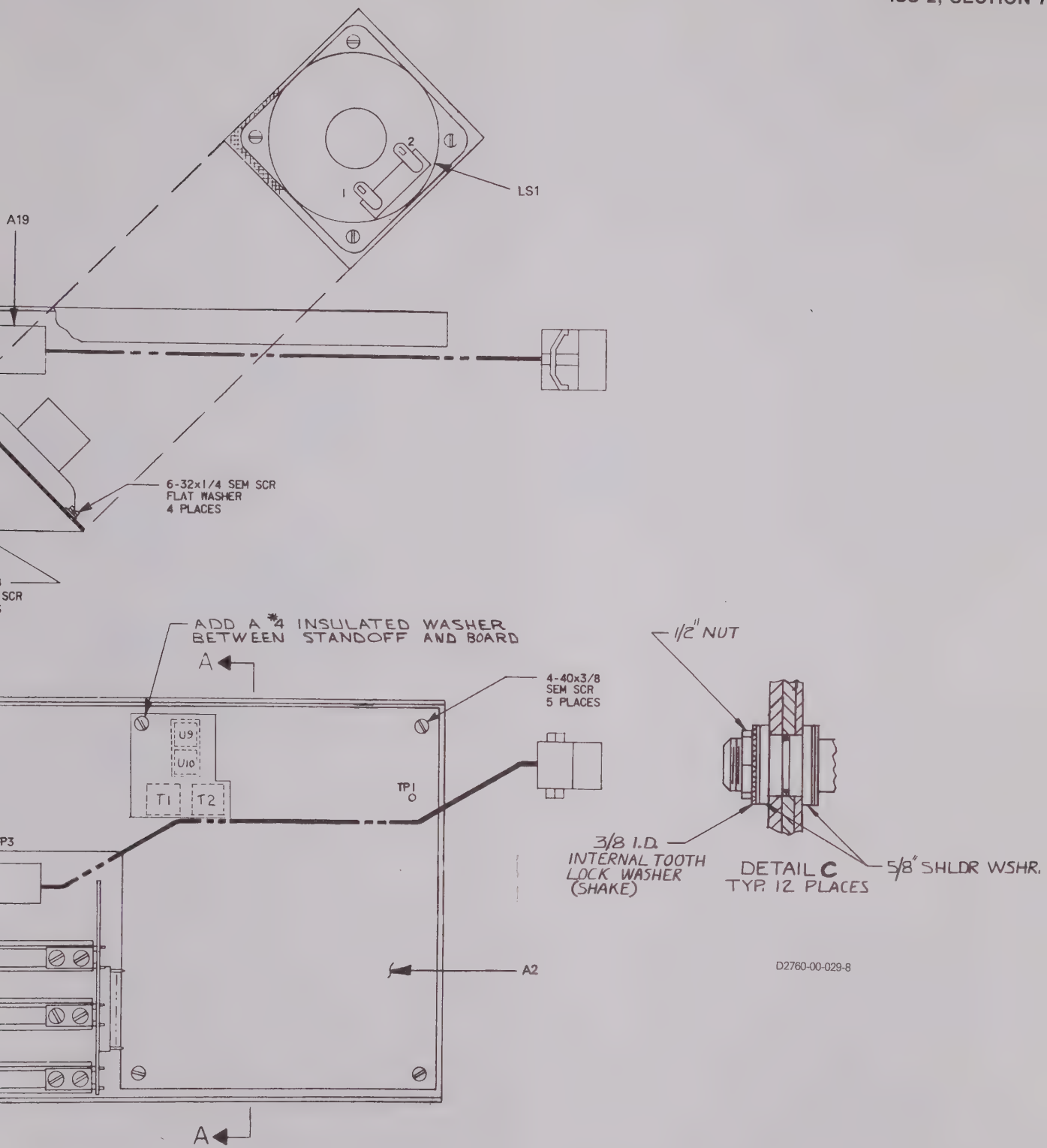
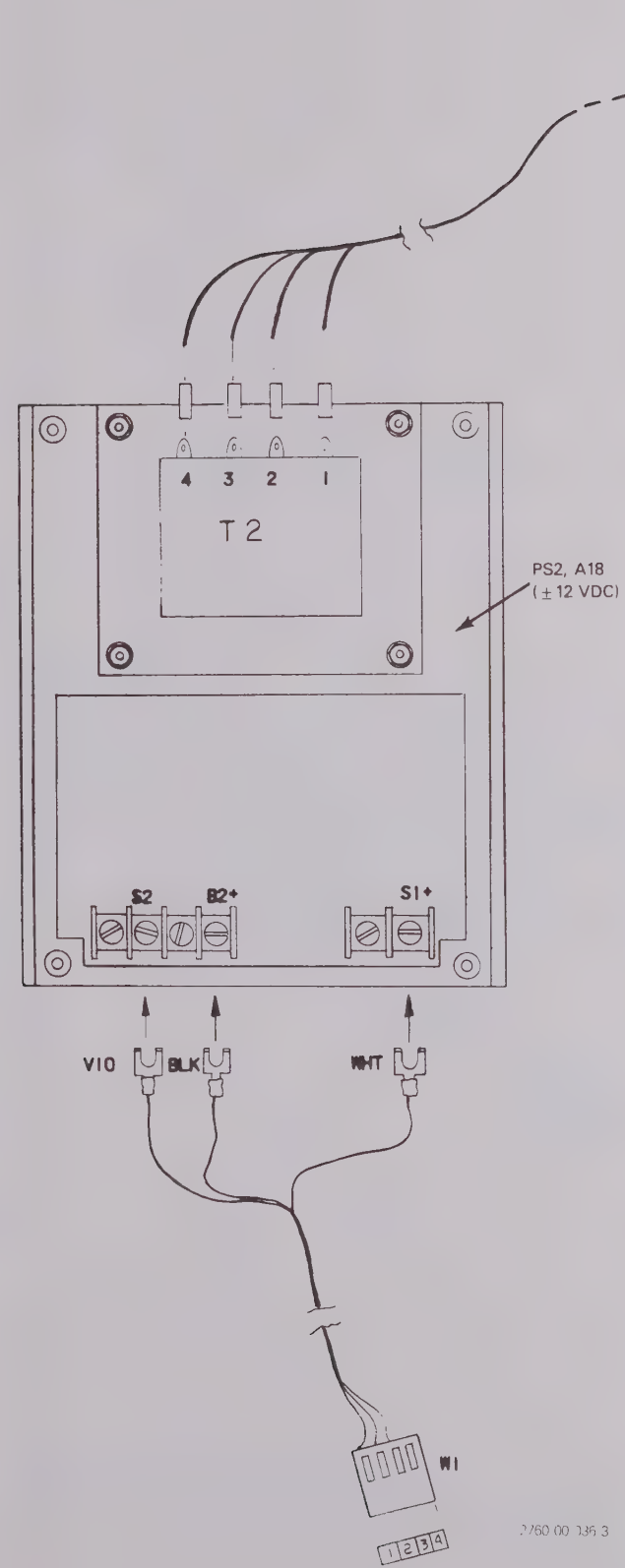


Fig. 25—Model 2760 Resident Module Assembly Diagram (A12)


4 3 2 1
T 2
PS2, A18
(±12 VDC)
S2
B2+
S1+
VIO
BLK
WHT
W1
1 2 3 4

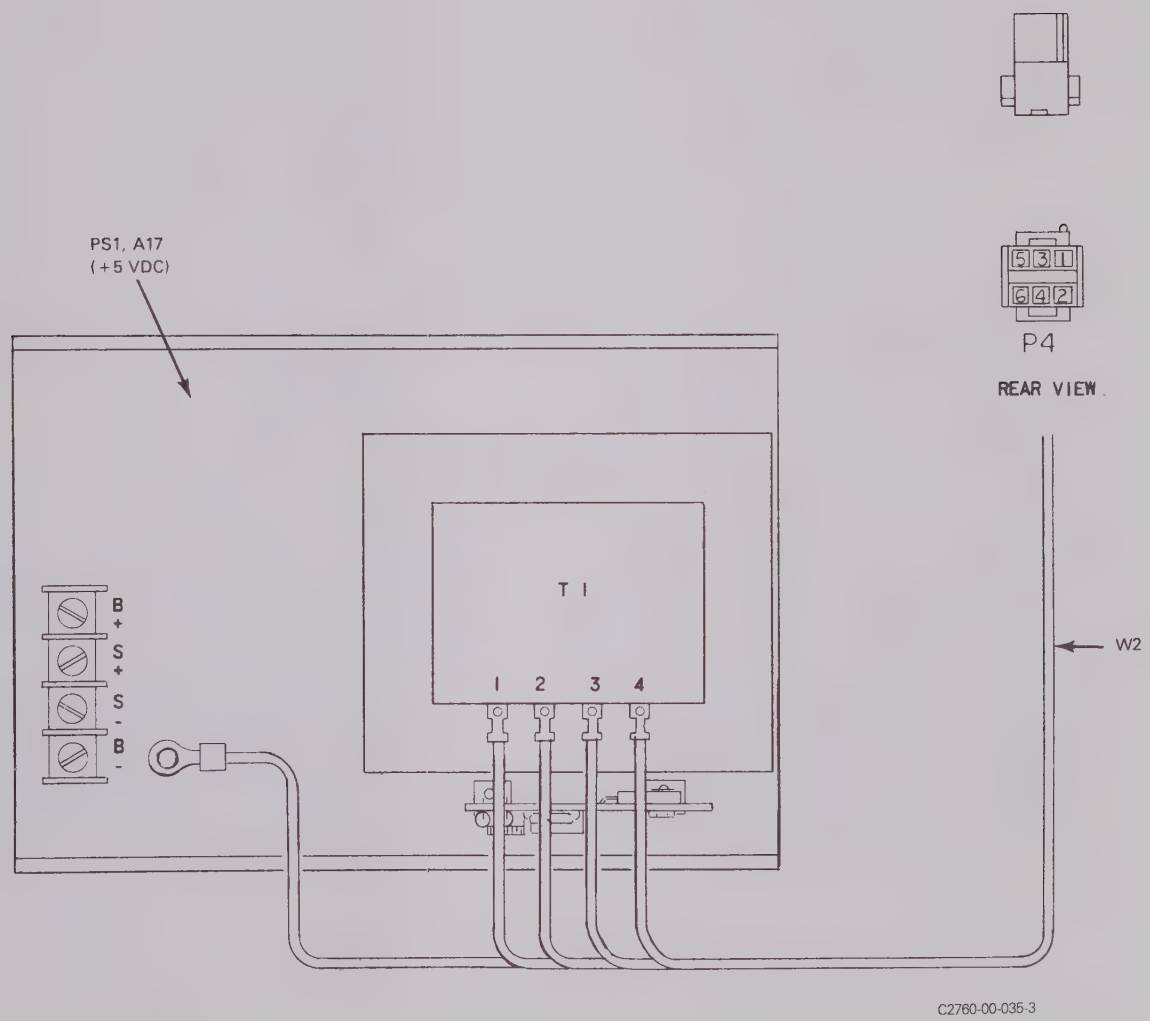


Fig. 27—Power Supply 1 and 2 Assembly Diagram (A17 and A18)

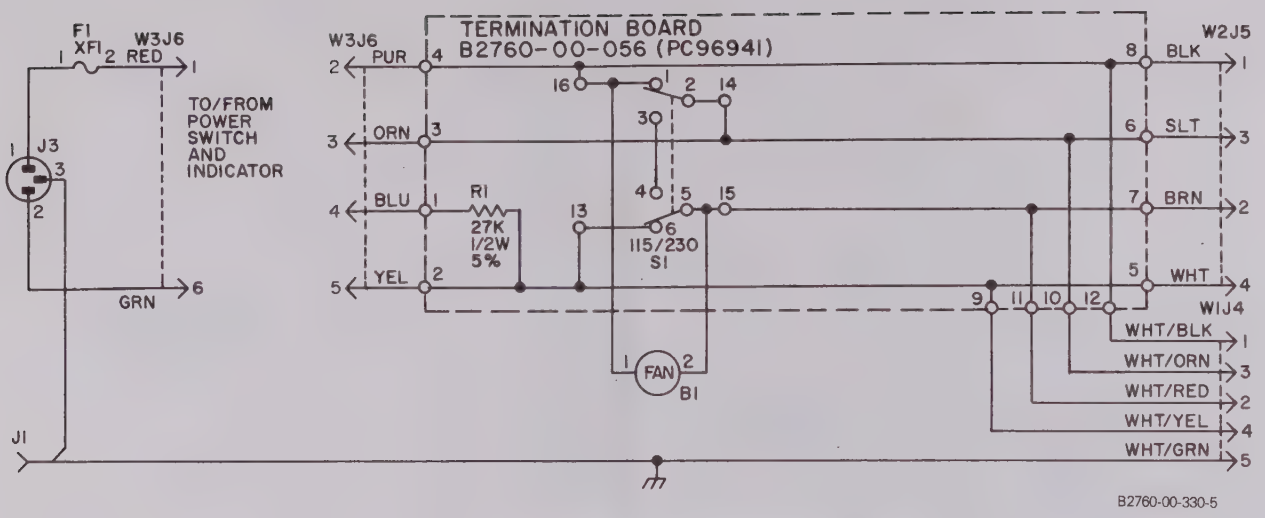


Fig. 29—Fan Housing (A14) Schematic Diagram

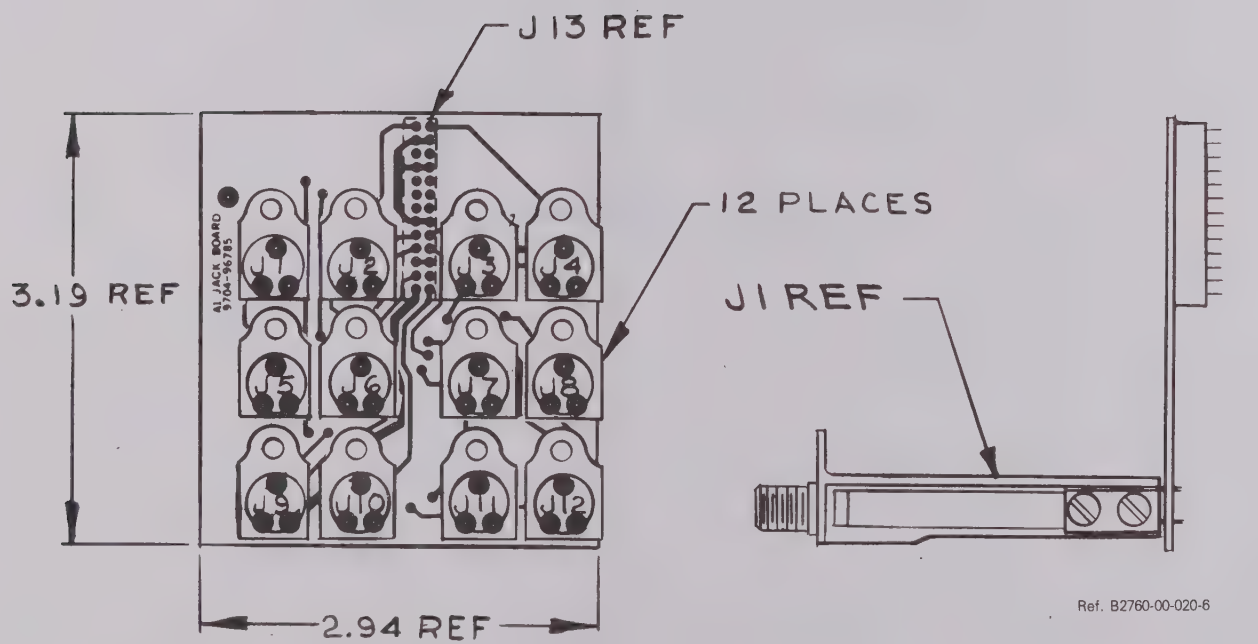
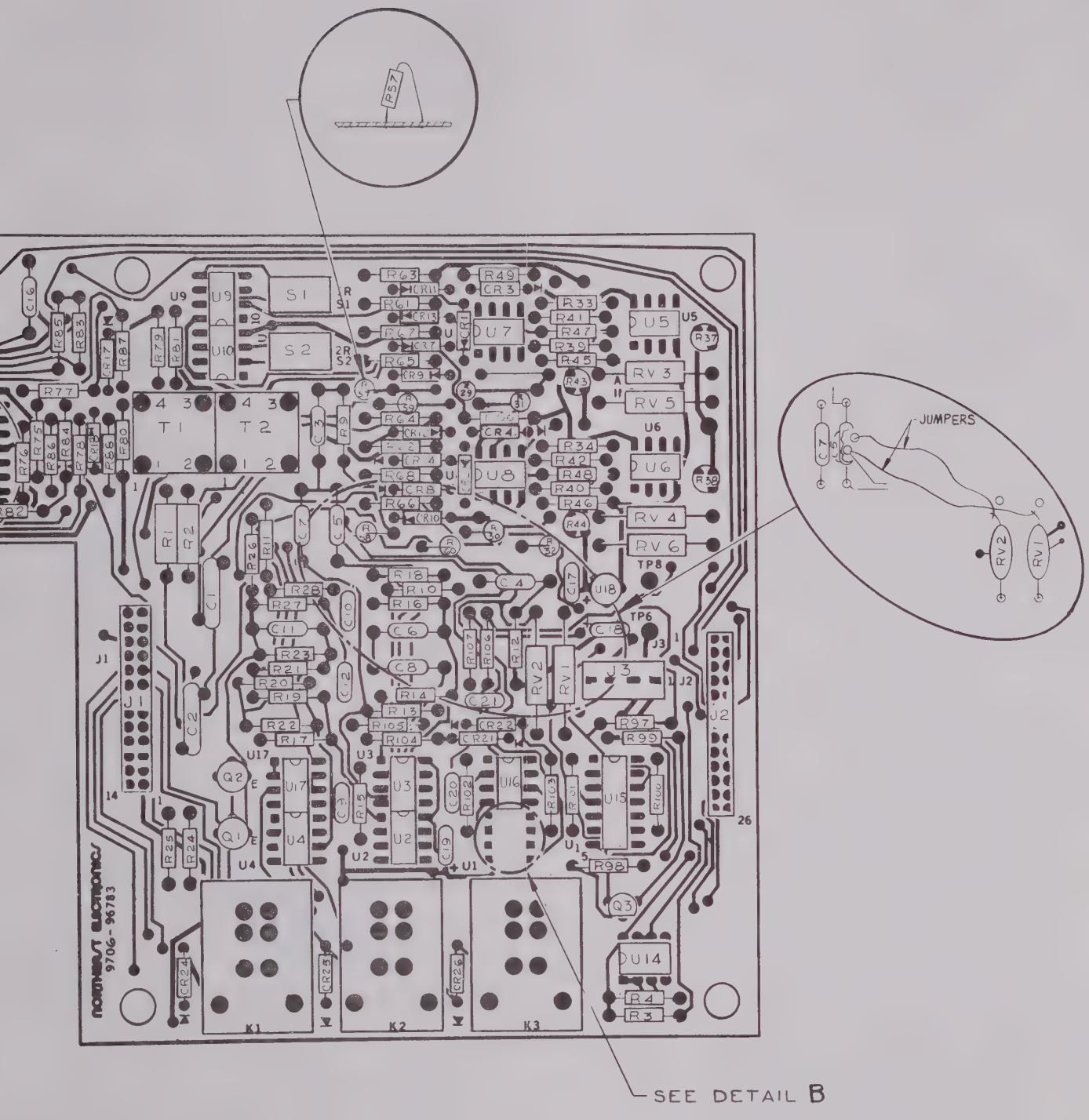
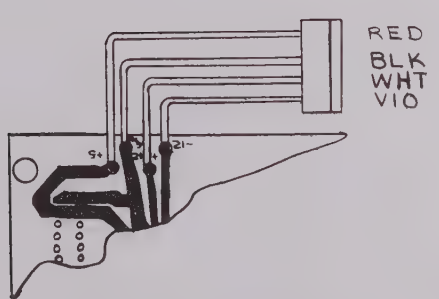


Fig. 30—Jack Board (A1) Parts Location Diagram



D2760 00-021 17

Fig. 32—Main Input Board (A2)
Parts Location Diagram



NON COMPONENT SIDE

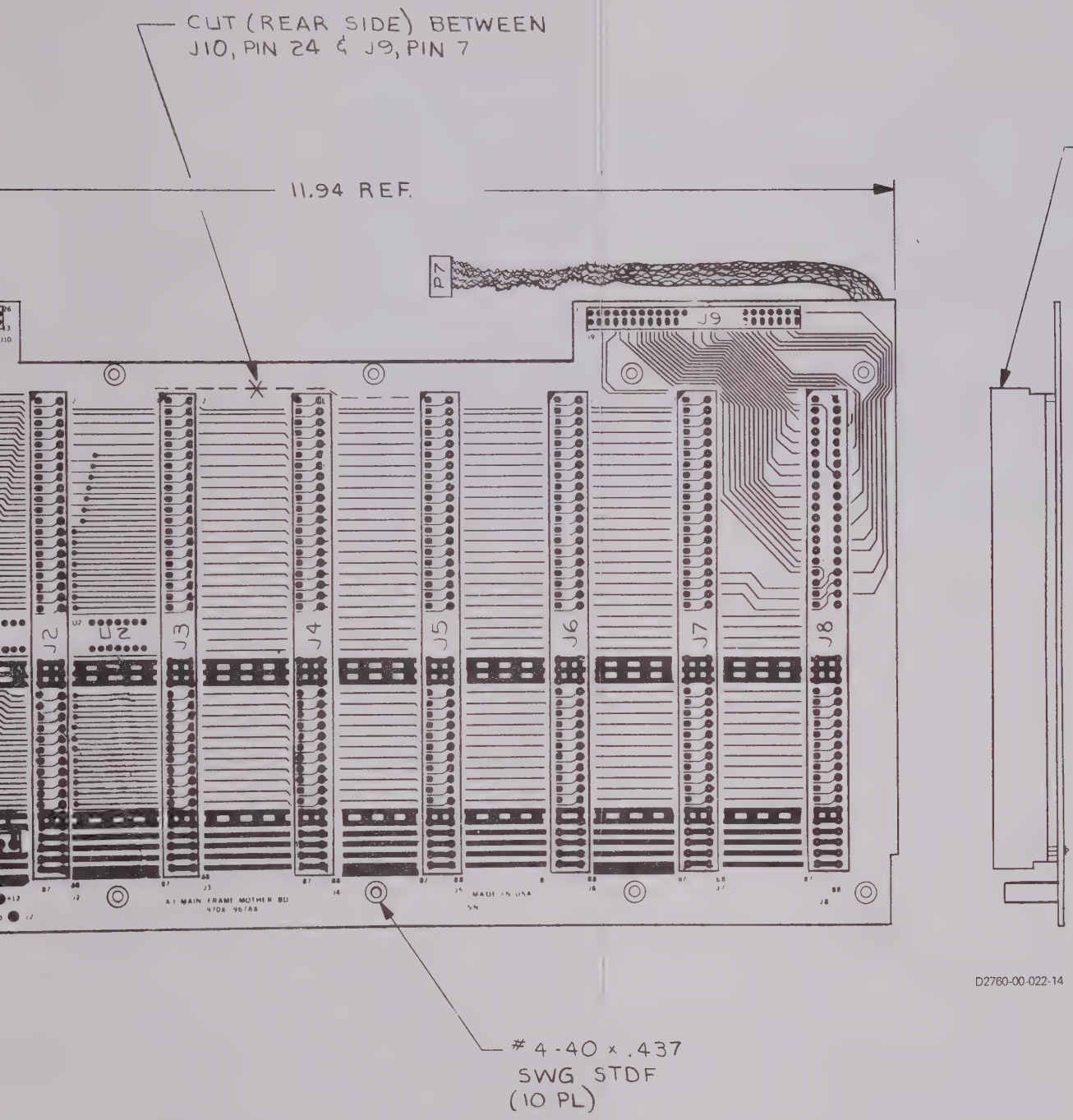
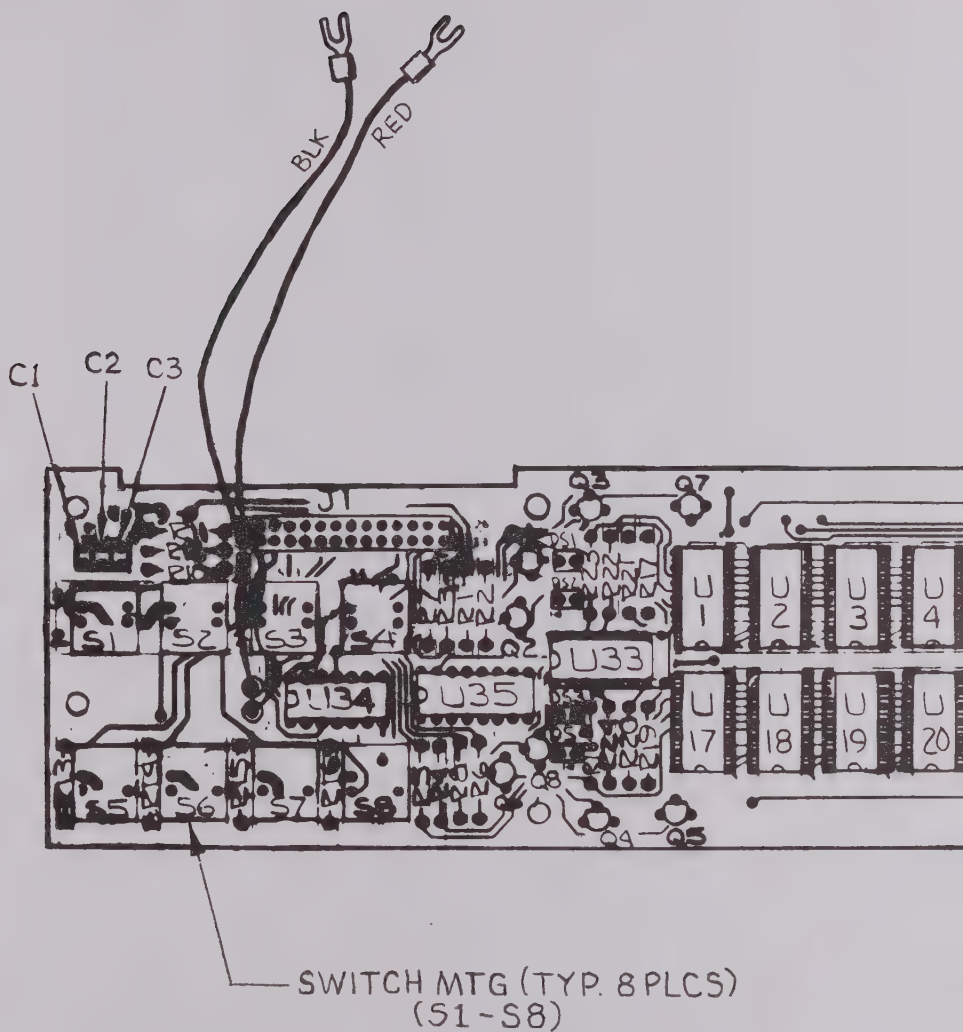


Fig. 34—Mainframe Mother Board (A3) Assembly Diagram


BLK
RED
C1
C2
C3
J1
S1
S2
S3
S4
S5
S6
S7
S8
U33
U134
U35
U1
U2
U3
U4
U17
U18
U19
U20
Q2
Q3
Q4
Q5
Q7
Q8
SWITCH MTG (TYP. 8 PLCS)
(S1-S8)

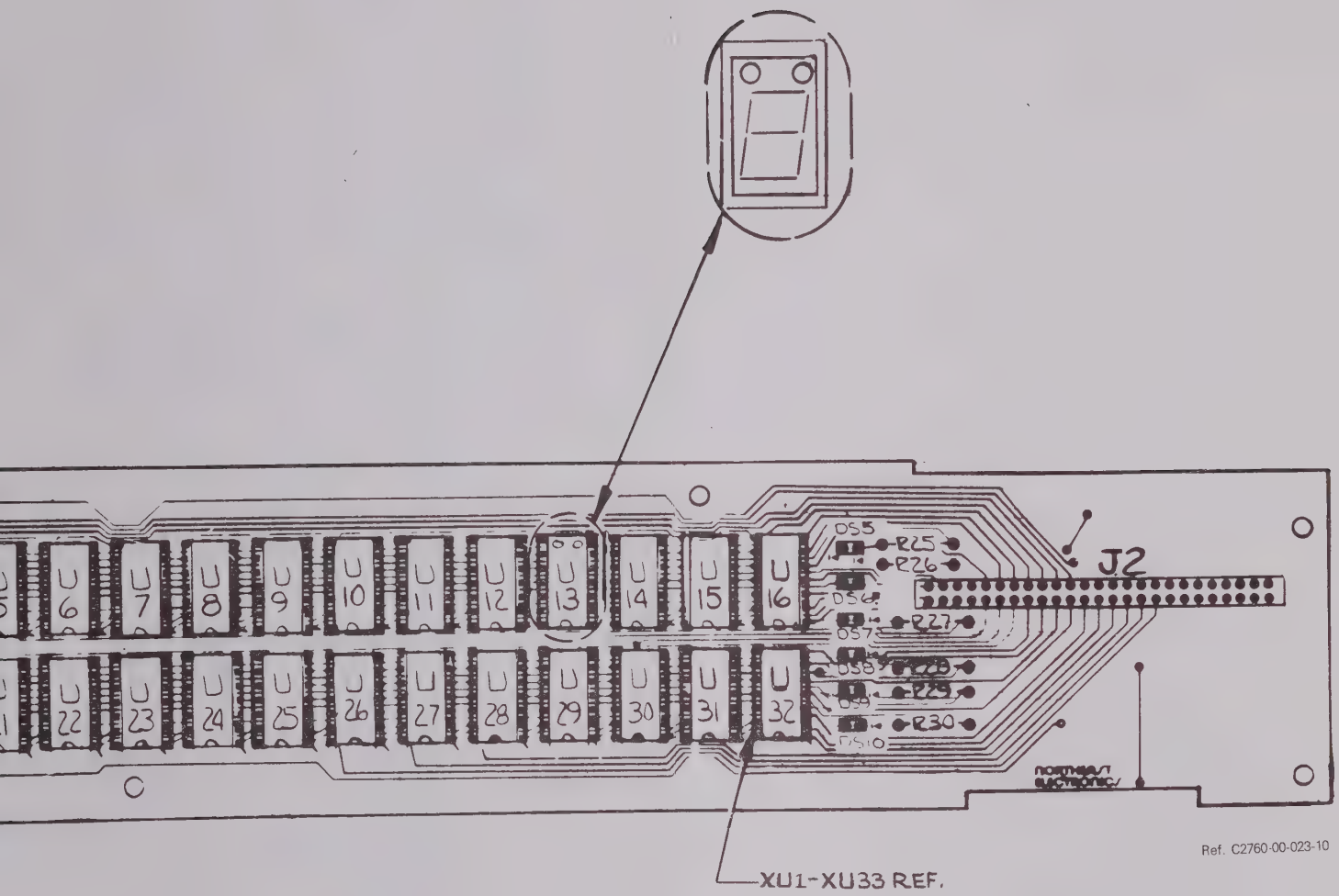
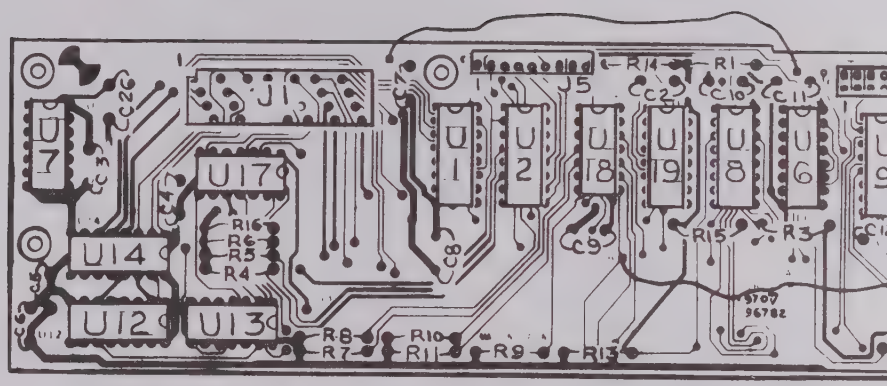
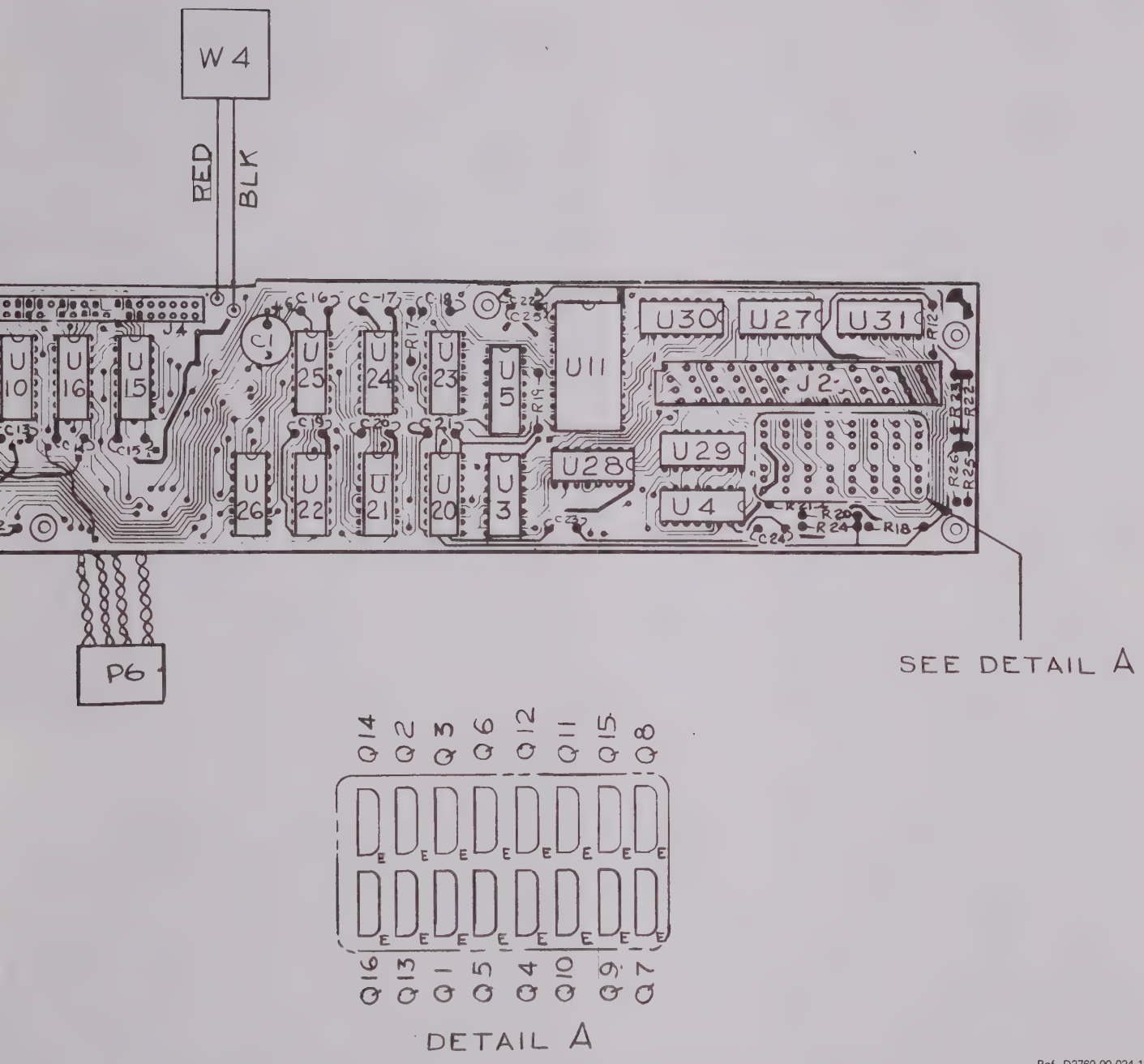


Fig. 36—Display Board (A4) Parts Location Diagram


J1
J5
U1
U2
U18
U19
U8
U6
U7
U17
U14
U12
U13
R16
R6
R5
R4
R8
R7
R10
R11
R9
R13
R15
R3
R14
R1
C2
C10
C11
C8
C9
C3
C4
C5
C6
9707
96782



Ref. D2760-00-024-13

Fig. 38—Display Driver (A5) Parts Location Diagram

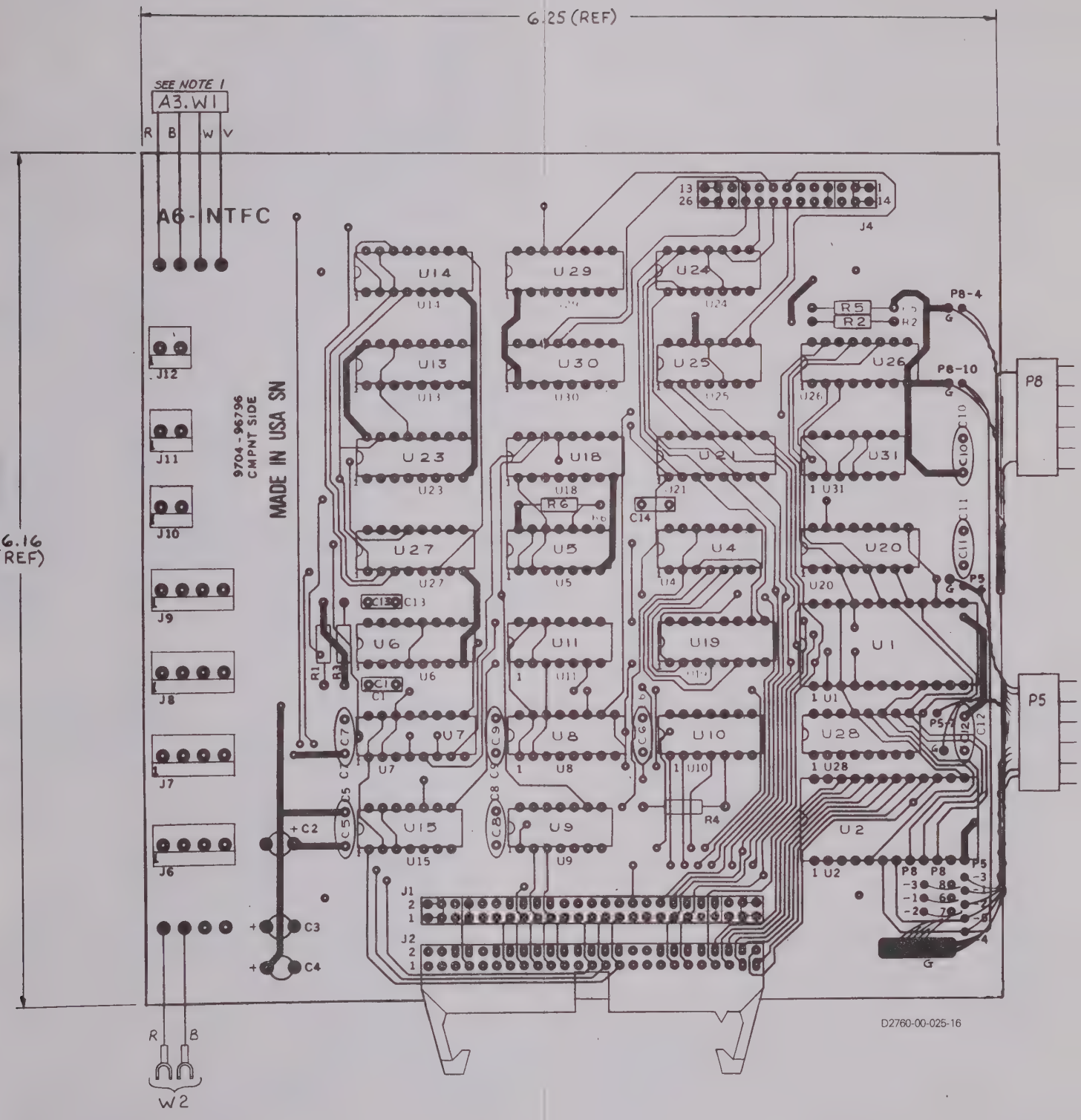


Fig. 40—Interface Board (A6) Parts Location Diagram

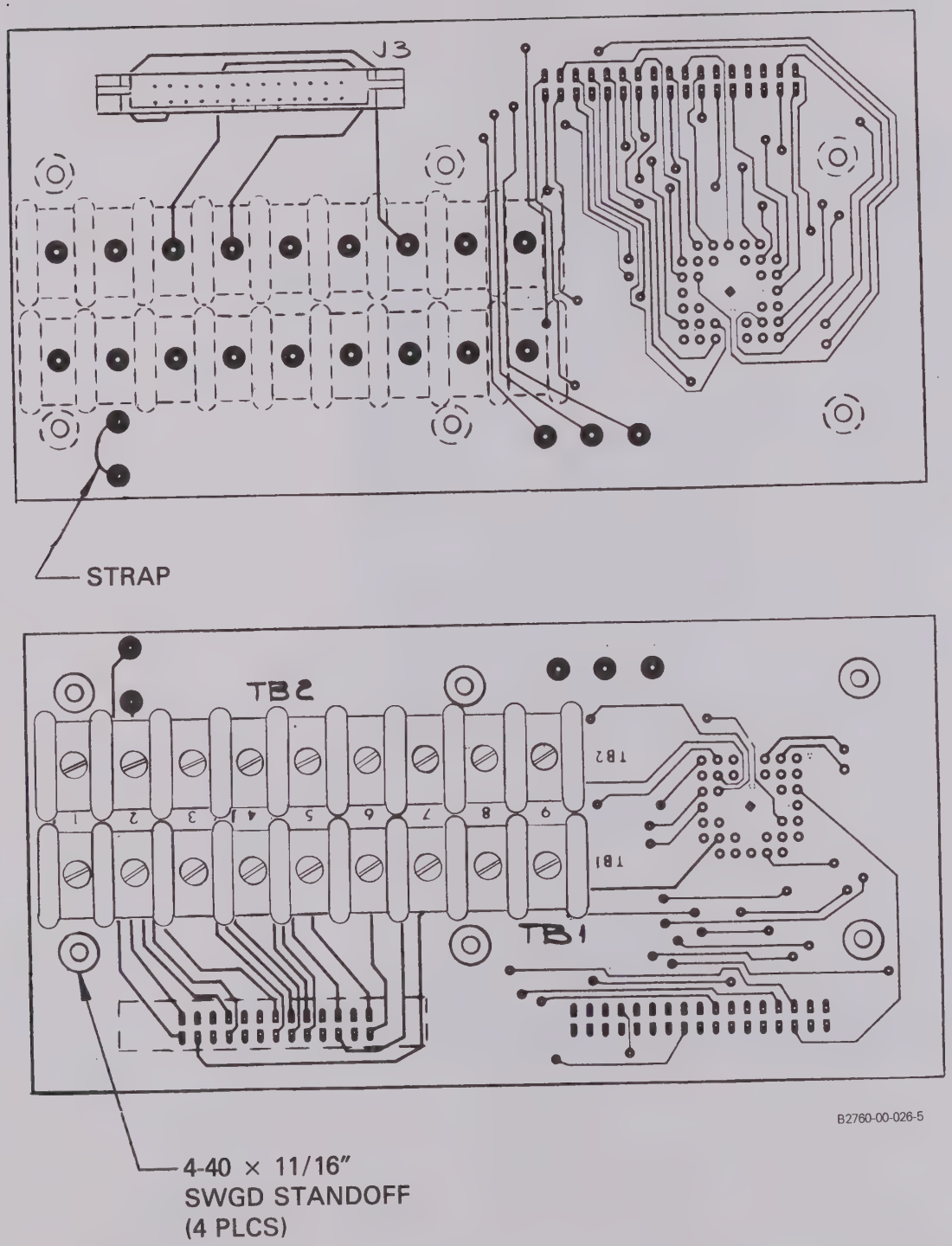


Fig. 42—Accessory Connection Board (A7) Parts Location Diagram

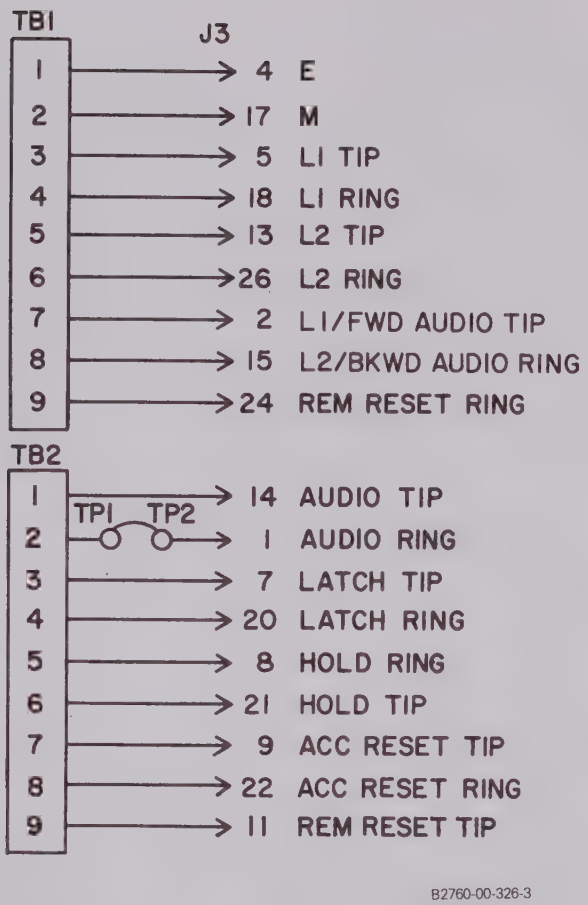
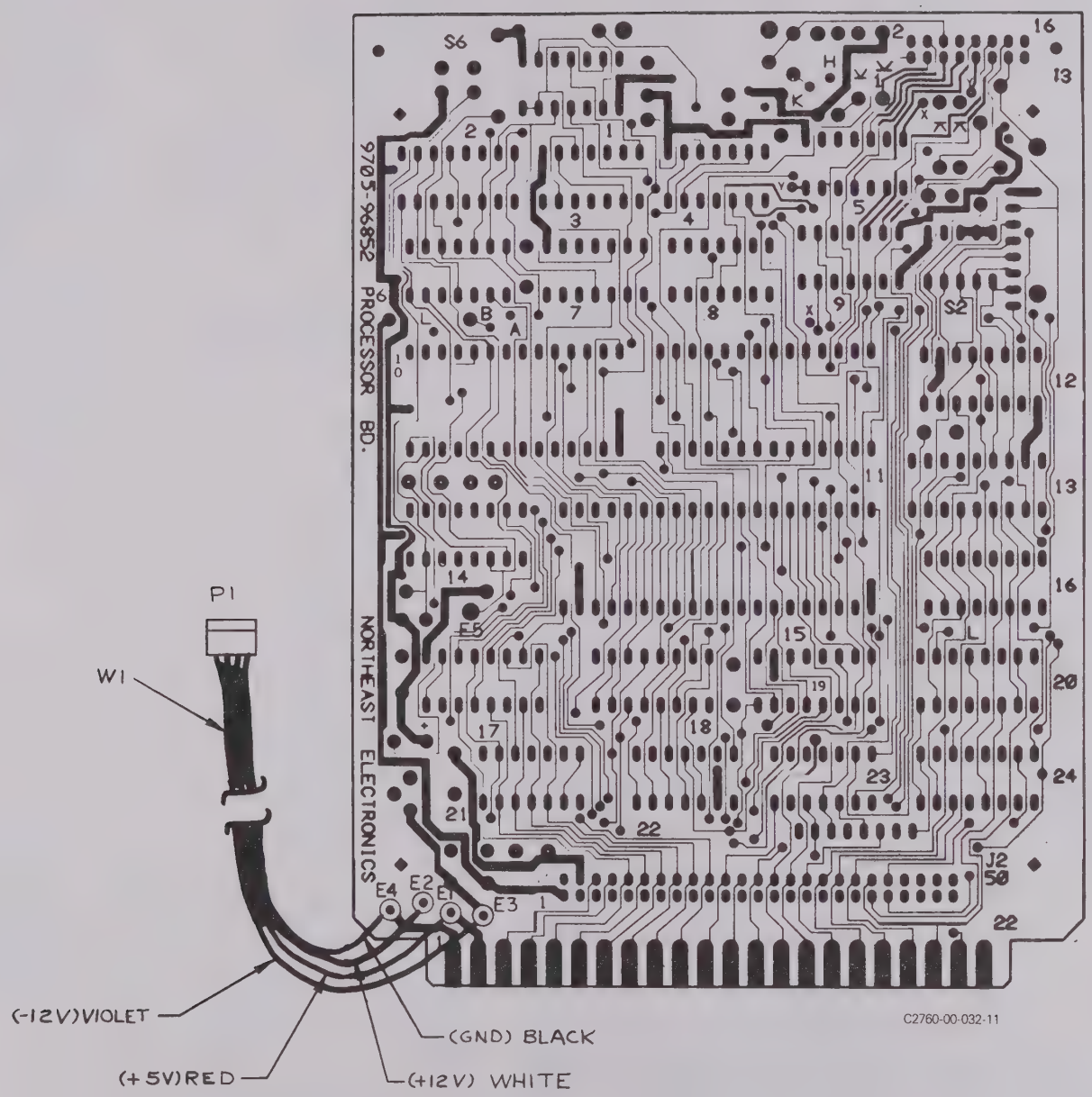
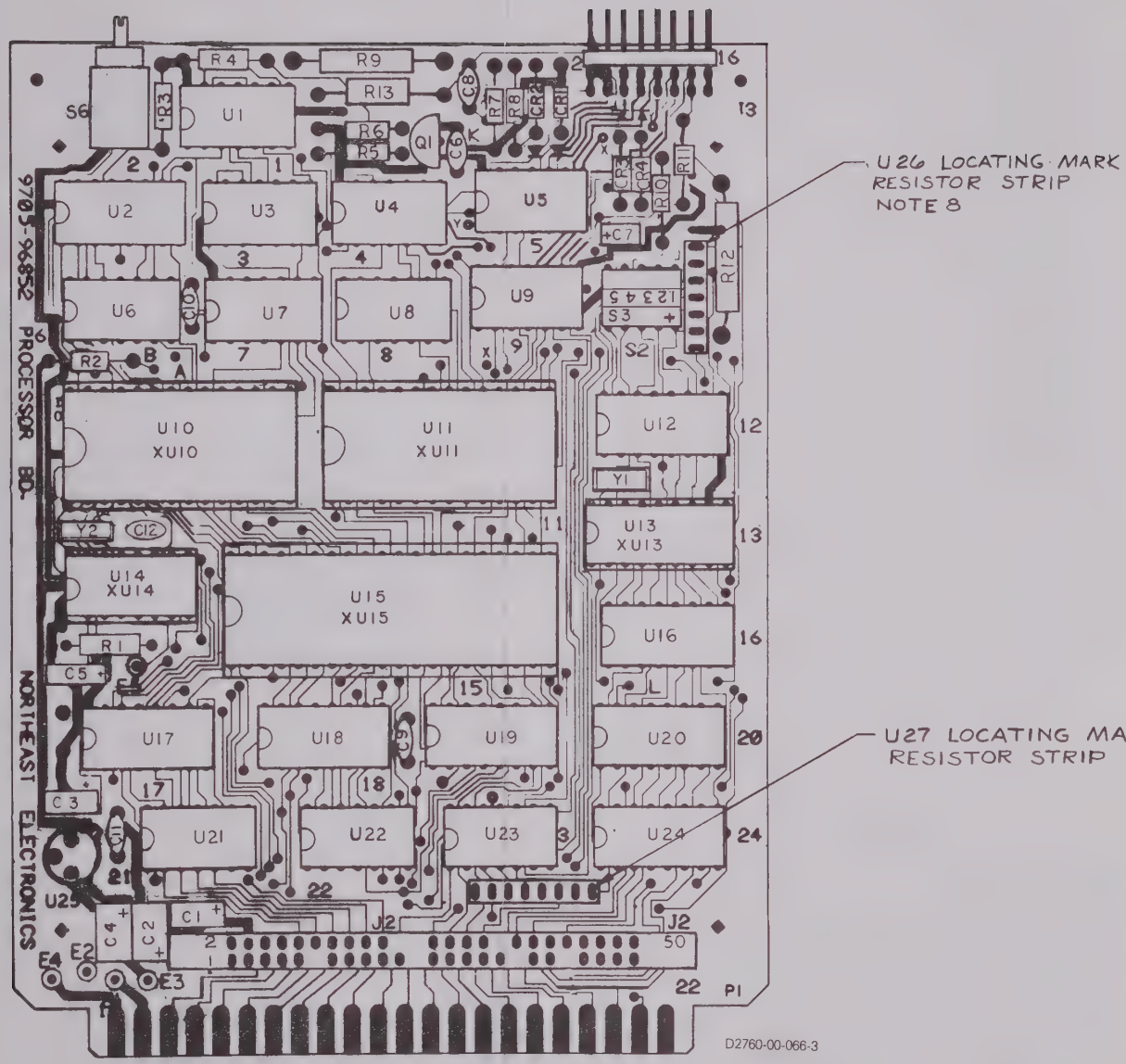

TB1
J3
1 → 4 E
2 → 17 M
3 → 5 L1 TIP
4 → 18 L1 RING
5 → 13 L2 TIP
6 → 26 L2 RING
7 → 2 L1/FWD AUDIO TIP
8 → 15 L2/BKWD AUDIO RING
9 → 24 REM RESET RING
TB2
TP1
TP2
1 → 14 AUDIO TIP
2 → 1 AUDIO RING
3 → 7 LATCH TIP
4 → 20 LATCH RING
5 → 8 HOLD RING
6 → 21 HOLD TIP
7 → 9 ACC RESET TIP
8 → 22 ACC RESET RING
9 → 11 REM RESET TIP
B2760-00-326-3

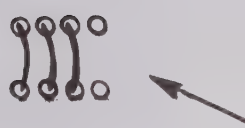
Fig. 43—Accessory Connection Board (A7) Schematic Diagram


S6
9705-96852
PROCESSOR BD.
NORTHEAST ELECTRONICS
S2
J2
50
P1
W1
E1
E2
E3
E4
E5
(-12V)VIOLET
(+5V)RED
(GND) BLACK
(+12V) WHITE
C2760-00-032-11



COMPONENT PLACEMENT

Fig. 44—8080 Processor Board (A8) Parts Location Diagram



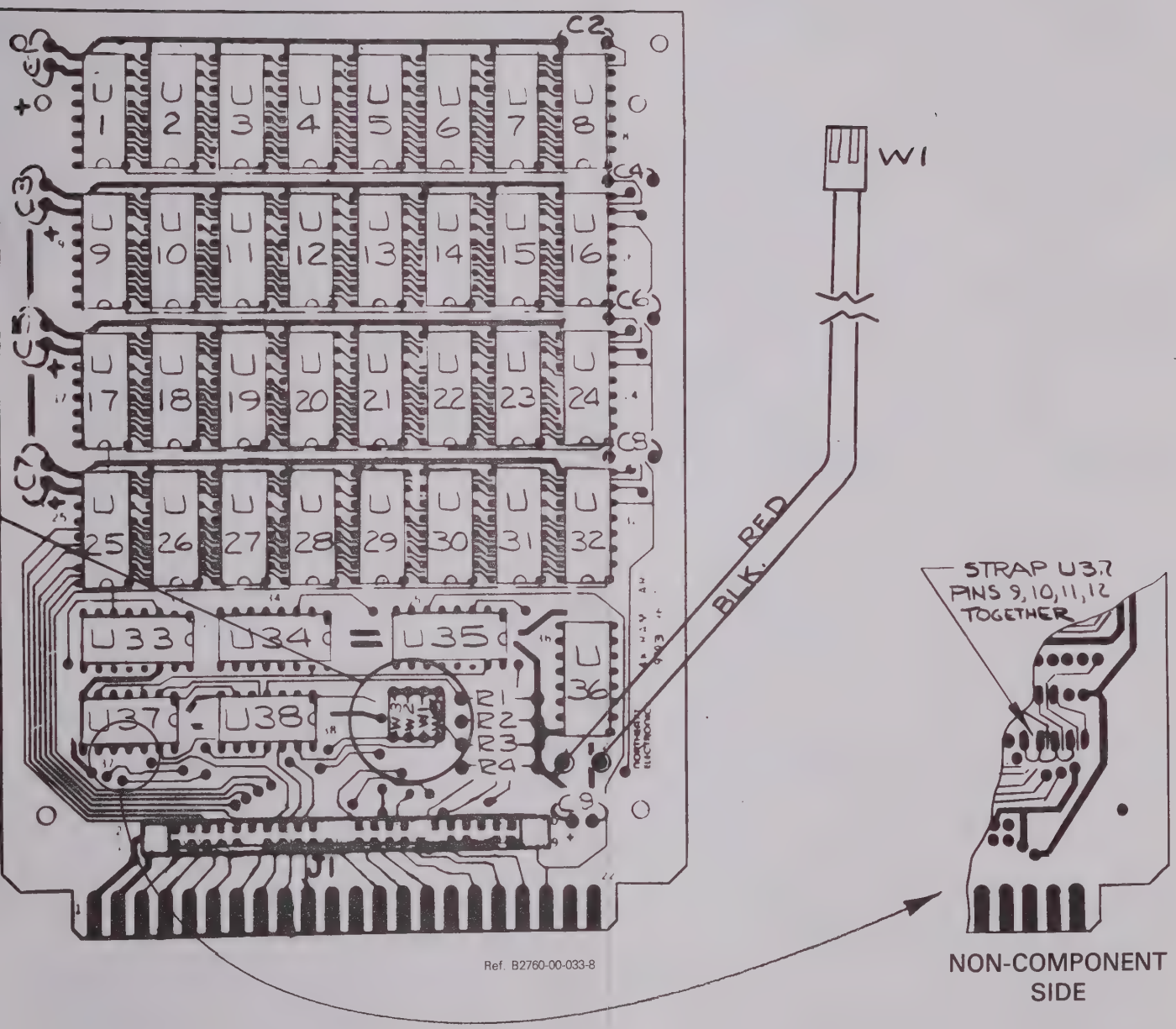


Fig. 46—4K RAM Board (A9) Parts Location Diagram

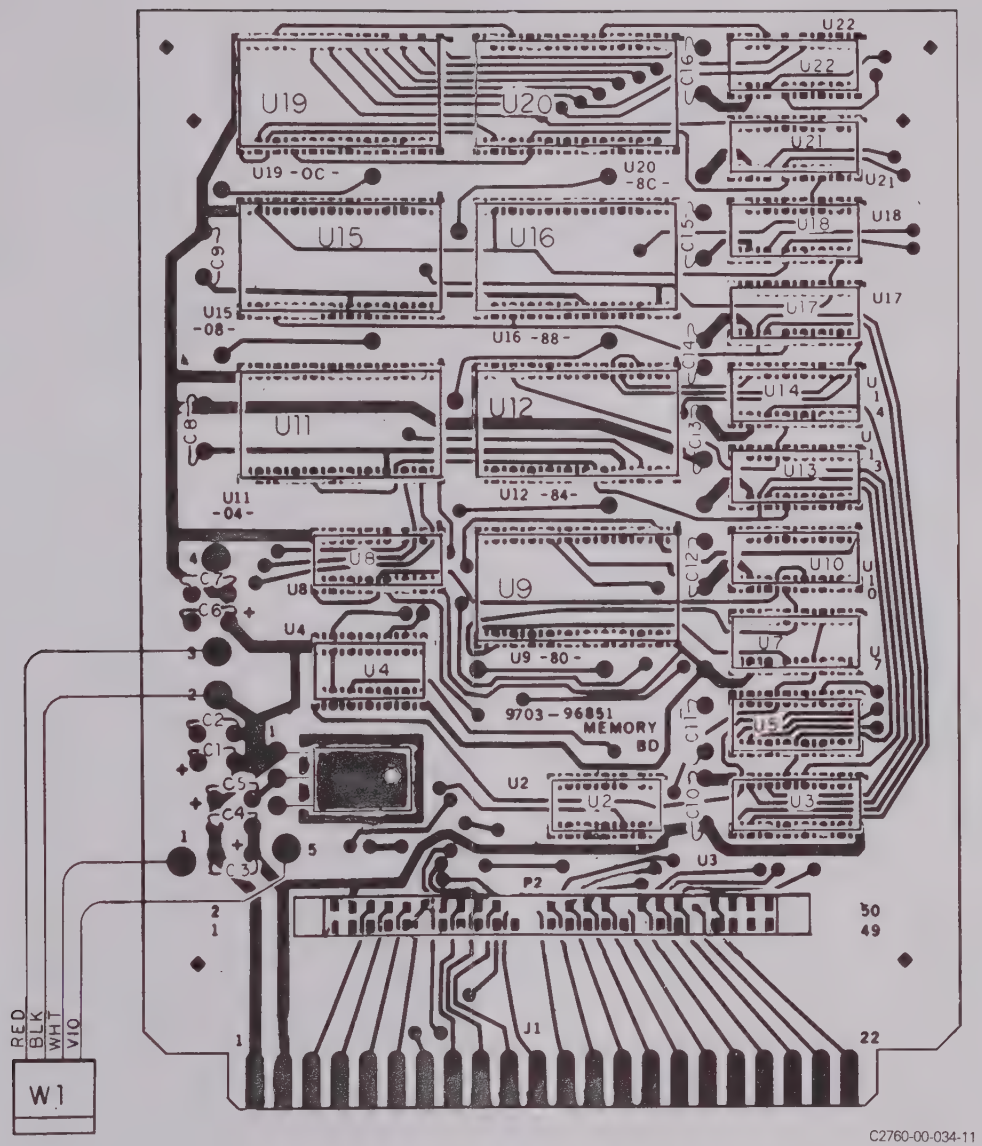
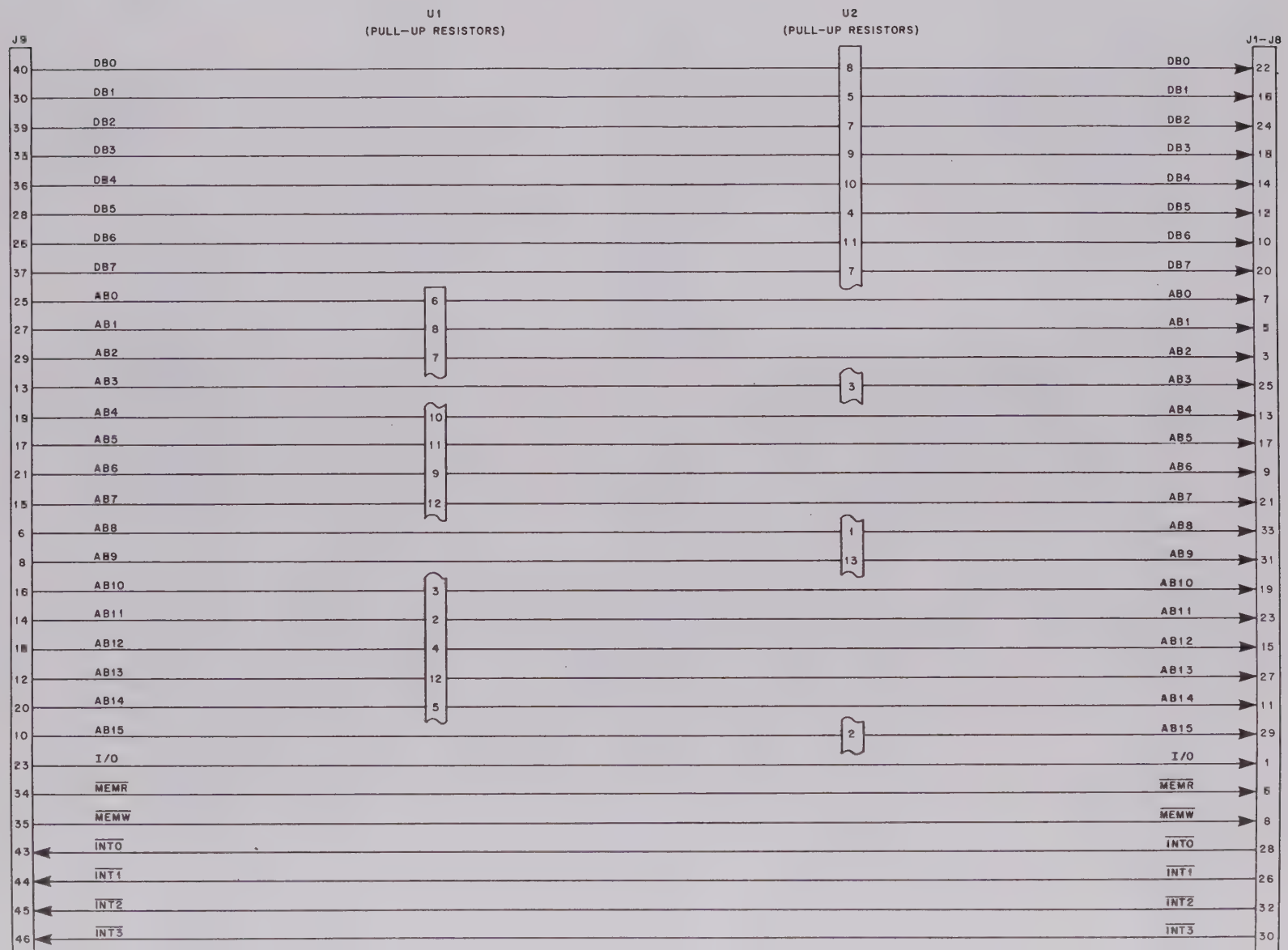


Fig. 48—ROM RAM Board (A10) Parts Location Diagram


U1
(PULL-UP RESISTORS)
U2
(PULL-UP RESISTORS)
J9
J1-J8
40 DB0
30 DB1
39 DB2
38 DB3
36 DB4
28 DB5
26 DB6
37 DB7
25 AB0
27 AB1
29 AB2
13 AB3
19 AB4
17 AB5
21 AB6
15 AB7
6 AB8
8 AB9
16 AB10
14 AB11
18 AB12
12 AB13
20 AB14
10 AB15
23 I/O
34 MEMR
35 MEMW
43 INT0
44 INT1
45 INT2
46 INT3
6 8 7
10 11 9 12
3 2 4 12 5
8 5 7 9 10 4 11 7
3
1 13
2
DB0 22
DB1 16
DB2 24
DB3 18
DB4 14
DB5 12
DB6 10
DB7 20
AB0 7
AB1 5
AB2 3
AB3 25
AB4 13
AB5 17
AB6 9
AB7 21
AB8 33
AB9 31
AB10 19
AB11 23
AB12 15
AB13 27
AB14 11
AB15 29
I/O 1
MEMR 5
MEMW 8
INT0 28
INT1 26
INT2 32
INT3 30

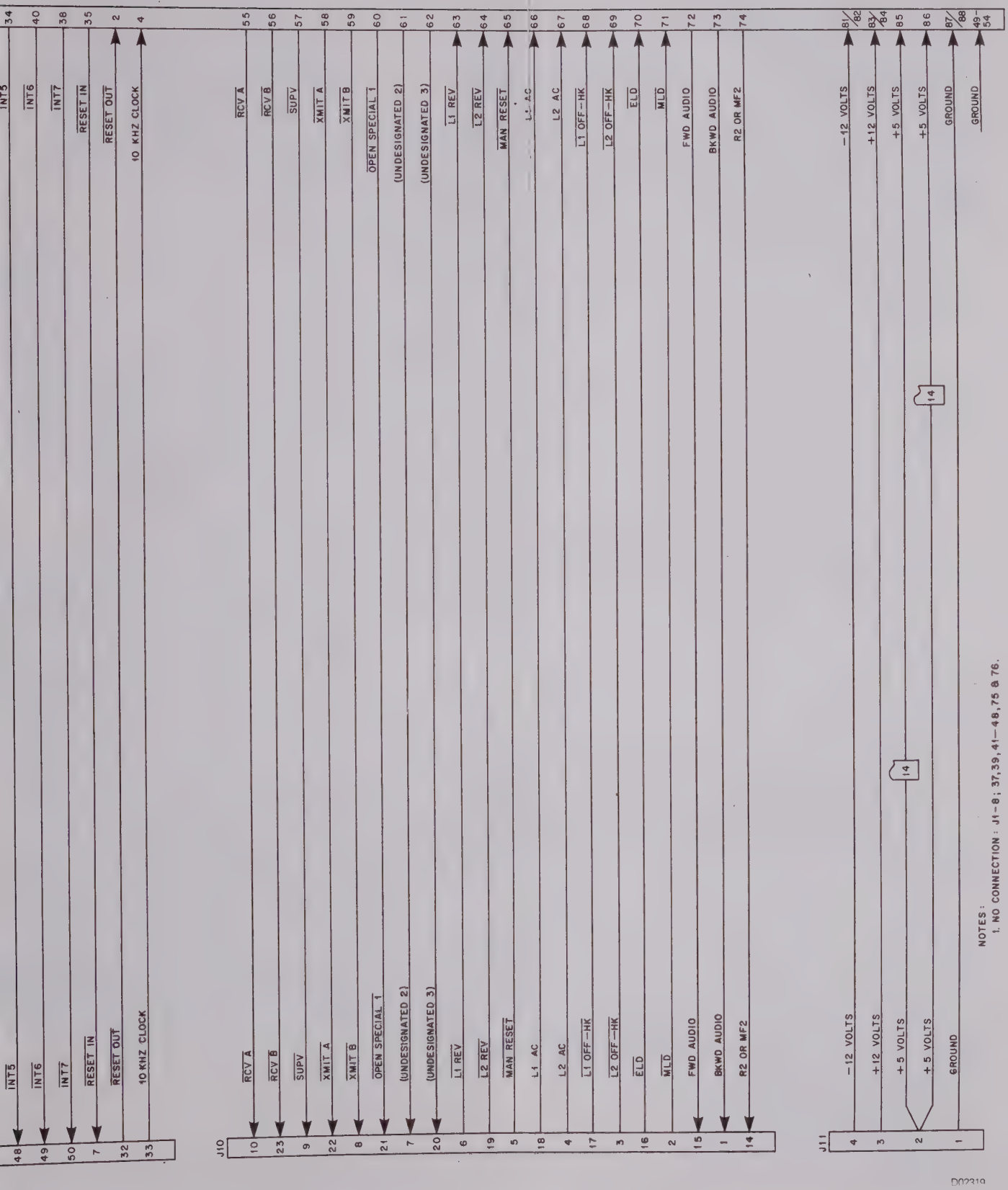


Fig. 50—Mainframe Mother Board (A3)

8. ELECTRONIC PARTS LISTS

A. General

8.01 Tables T through KK list the electronic parts for the Model 2760 Universal Signaling Analyzer mainframe. The component location diagrams contained in Part 7 show reference designations and locations for all electronic parts.

Table T. Model 2760 Mainframe Parts List

A2760-00-001
REV 16 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
A3	INTERCONNECT P.C. ASSY	A276000060
A6	PC ASSY.96796 INTERFCE A6	A276000025
A7	PC ASSY.96794 ACC-CON A7	A276000026
A8	ASSY, PROCESSOR W/CABLE	A276000032
A9	PC ASSY 96773 4K RAM	A276000033
A10	PC ASSY 96851 ROM RAM	A276000034
A12	RESIDENT MODULE ASSY	A276000029
A13	DISPLAY ASSY	A276000028
A14	FAN HOUSING ASSY	A276000030
A15	CASE WELDMENT	A276000202
A17	CABLE PS1	A276000035
A18	CABLE PS2	A276000036
W2	CABLE JACK-MAIN-ACC.	A276000013
W3	CABLE MAIN INTERCONN INTF	A276000012
W5	CABLE CPU	A276000014

Table U. Resident Module Assembly (A12) Parts List

A2760-00-029
REV 08 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC		PART NO.
A1	PC ASSY.96785 JACK BD A1			A276000020
A2	MAIN INPUT P.C. ASSY			A276000021
A19	CABLE PWR SW			A276000037
LS1	SPEAKER 45 OHM			926000200
R1	POTNTMTR CON-PLAS1K-1K	VRES.523 N	1/2W 10% LIN CONCEN	238001027
S2	SWITCH TOGGLE SPDT		ON-NONE-ON GOLD	620400100

Table V. Display Assembly (A13) Parts List

A2760-00-028
REV 08 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION		PART NO.
A4	PC ASSY.96781 DISPLAY A4		A276000023
A5	PC ASSY.96782 DRIVER A5		A276000024
S9	KEYPAD 4X4	*	635000301
W4	CABLE DVR INTFC INTERCONN		A276000019
W5	CABLE KEYPAD-DISP.DRIVER		A276000017

Table W. Power Supply PS1 (A17) Parts List

A2760-00-035
REV 03 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION		PART NO.
PS1	PWR-SPLY AC-DC LN 115/230	45W 5V,2X15V/OVP	960104008
W2	CABLE PS1.W2		A276000046

Table X. Power Supply PS2 (A18) Parts List

A2760-00-036
REV 03 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION		PART NO.
PS2	PWR-SPLY AC-DC LN 115/230	25W -12V,+12V/ OVP	960104007
W1	CABLE-PS2 DC		A276000039
W2	CABLE PS2.W2		A276000047

Table Y. Fan Housing (A14) Parts List

A2760-00-030
REV 05 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION				PART NO.
A1	PC 96941 TERMINATION				A276000056
B1	FAN	AXIAL	35 CGM	15W 115V	920001000
F1-2	FUSE	GLASS	3AG 2A	125V SLOW	863101700
J1	POST	BINDING		METAL GND	652500100
J3	RECEPTCL	PANEL	3 PIN	6A 250	652201700
S1	SWITCH	SLIDE	DPDT	LOCKING	645500200
W1	CABLE A14.W1				A276000049
W2	CABLE A14.W2				A276000050
W3	CABLE A14.W3				A276000051
XF1-2	FUSEHLDR	PANEL	3AG		863000100

Table Z. Jack Board (A1) Parts List

A2760-00-020
REV 06 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
J1-12	JACK TELEPHNE 3COND 3TERM W-WRAP .25"	650403700
J13	CONNECTR HEADER 26 DIL GOLD STRAIGHT	654003323

Table AA. Main Input Board (A2) Parts List

A2760-00-021
REV 17 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
A1	GAIN ADAPTER BD	A276000058
A2	BOARD,MAIN INPUT	970696783
C1-2	CAPACITR POLYESTR 27 NF CAP.043 P 100V 10%	320002730
C3-4	CAPACITR POLYESTR 22 NF CAP.043 F 100V 10%	320002230
C5-6	CAPACITR POLYESTR 2.2 NF CAP.043 F 100V 10%	320002220
C7-8	CAPACITR POLYESTR 22 NF CAP.043 F 100V 10%	320002230
C9-10	CAPACITR CERAMIC 1.0 UF CAP.037 F 50V 20% Z5U	330801050
C11	CAPACITR POLYESTR 1.0 NF CAP.043 F 100V 10%	320001020
C12	CAPACITR CERAMIC 1.0 UF CAP.037 F 50V 20% Z5U	330801050
C13-14	CAPACITR POLYESTR 3.3 NF CAP.043 F 100V 10%	320003320
C15-16	CAPACITR POLYESTR 47 NF CAP.043 F 100V 10%	320004730
C17	CAPACITR ELECT-TA 2.2 UF CAP.036 F 35V 10%	310002250
C18	CAPACITR ELECT-TA 1.0 UF CAP.036 F 35V 10%	310001051
C19	CAPACITR ELECT-TA 8.2 UF CAP.036 F 15V 10%	310008250
C20-21	CAPACITR CERAMIC 10 NF CAP.082 F 16V 20% Y5P	330701031
CR1-22	DIODE SIGNAL 1N4148 RES.001 75V SI 4.0NS	560041480
CR24-26	DIODE SIGNAL 1N4148 RES.001 75V SI 4.0NS	560041480
DS1-6	LED T1.75RED 5.0V LED.001 16MA 60DEG 1MCD RES	564500800
J1-2	CONNECTR HEADER 26 DIL GOLD STRAIGHT	654003323
J3	LOCK FRICTION 4 CKT RND-WIRE CNTR-WAFR	654003603
K1-3	RELAY INDUSTRL 12V 1A F AG 10A 160R PC	604100450
Q1	TRANSSTR BJT-NPN 2N2102 TO5.01 65V SI HFE40 1A	550021020
Q2	TRANSSTR BJT-PNP 2N4036 TO5.01 65V SI HFE20 1A	552040360
Q3	TRANSSTR BJT-NPN MPS6515 TO92.001 25V SI HFE250 0.1A	550065150
R1-2	RESISTOR MTL-FILM 22.6 K RES.006 P .75W 1% 100PPM 350V	220622691
R3-4	RESISTOR CARBON 10 K RES.001 F 1/4W 10%	200101036
R9-10	RESISTOR CARBON 4.7 K RES.001 F 1/4W 10%	200104726
R11-12	RESISTOR MTL-FILM 17.8 K RES.001 P .25W 1% 100PPM 250V	220217821
R13-14	RESISTOR MTL-FILM 383 K RES.001 P .25W 1% 100PPM 250V	220238331
R15-16	RESISTOR MTL-FILM 11.0 K RES.001 P .25W 1% 100PPM 250V	220211021
R17-18	RESISTOR CARBON 33 K RES.001 F 1/4W 10%	200103336
R19-20	RESISTOR CARBON 1.0 K RES.001 F 1/4W 10%	200101026
R21-22	RESISTOR MTL-FILM 30.1 K RES.001 N .25W 1% 100PPM 250V	220230121
R23	RESISTOR CARBON 100 K RES.001 F 1/4W 10%	200101046
R24-25	RESISTOR CARBON 39 R RES.001 F 1/4W 10%	200103906
R26	RESISTOR CARBON 47 R RES.001 F 1/4W 10%	200104706
R27	RESISTOR CARBON 3.3 K RES.001 F 1/4W 10%	200103326
R28	RESISTOR CARBON 1.8 K RES.001 F 1/4W 10%	200101826
R29-32	RESISTOR CARBON 470 K RES.004 F 1W 10%	200304746
R33-34	RESISTOR MTL-FILM 2.00 K RES.001 N .25W 1% 100PPM 250V	220220011

Table AA. (Cont)

A2760-00-021
REV 17 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
R37-38	TRIM-POT	CERM-1T	10	K	VRES.011	F	1/2W 10% TOP-ADJ	232701036
R39-42	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R43-44	TRIM-POT	CERM-1T	10	K	VRES.011	F	1/2W 10% TOP-ADJ	232701036
R45-48	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R49-50	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R51-52	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R57-60	RESISTOR	CARBON	470	K	RES.004	F	1W 10%	200304746
R61-62	RESISTOR	CARBON	1.0	M	RES.001	F	1/4W 10%	200101056
R63-64	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R65-66	RESISTOR	CARBON	4.7	M	RES.001	F	1/4W 10%	200104756
R67-68	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R69-70	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R75-78	RESISTOR	CARBON	220	K	RES.001	F	1/4W 10%	200102246
R79-80	RESISTOR	MTL-FILM	2.00	K	RES.001	N	.25W 1% 100PPM 250V	220220011
R81-82	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R83-84	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R85-86	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R87-88	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R89-90	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R91-92	RESISTOR	CARBON	1.0	K	RES.001	F	1/4W 10%	200101026
R97	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R98	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R99-101	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R102-103	RESISTOR	CARBON	47	K	RES.001	F	1/4W 10%	200104736
R104-105	RESISTOR	CARBON	470	R	RES.001	F	1/4W 10%	200104716
R106-107	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
RV1-6	VARISTOR	SILICON	SV-1					565510000
S1-2	SWITCH	SLIDE	DPDT				PC MOUNT	645500900
T1-2	TRANSFMR	AUDIO	P25K		XFMR.013	N	S600	400100801
U2-10	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U11	INT-CKT	TRANSSTR	3081		DIP.16	N	7 NPN COM EMIT	500030810
U12-13	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U14	INT-CKT	DRIVER	75451		DIP.8	N	MEM & PERPH DUAL	510075451
U15	INT-CKT	CMOS	4066		DIP.14	P	4 BILAT SWTCH	510004066
U16	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U17	INT-CKT	DRIVER	75451		DIP.8	N	MEM & PERPH DUAL	510075451
U18	INT-CKT	VOLT-REG	7905			N	FIXED NEG 500MA	500003201

Table BB. Interconnection Board (A3) Parts List

A2760-00-060
REV 00 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION				PART NO.
A3	PC ASSY.96788 INTERCON.A3				A276000022
U1-2	RESISTOR NETWORK	13X2K	DIP.14	100V 2%	514500100

Table CC. Display Board (A4) Parts List

A2760-00-023
REV 10 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
C1-3	CAPACITR	ELECT-TA	22 UF	CAP.036	F	6V 10%	310002260
DS1-10	LED	RECT-RED	2.5V			.1CNTR 30MA 2MCD	564501100
J1	CONNECTR	HEADER	26 DIL			GOLD STRAIGHT	654003323
J2	CONNECTR	HEADER	50 DIL			GOLD STRAIGHT	654003311
Q1-8	TRANSSTR	BJT-PNP	MPS6519	TO92.001		25V SI HFE250 0.1A	552065190
R1-8	RESISTOR	CARBON	470 R	RES.001	F	1/4W 10%	200104716
R9-16	RESISTOR	CARBON	10 K	RES.001	F	1/4W 10%	200101036
R17-24	RESISTOR	CARBON	100 R	RES.001	F	1/4W 10%	200101016
R25-30	RESISTOR	CARBON	47 R	RES.001	F	1/4W 10%	200104706
S1	SWITCH	PUSH-BTN					635800701
S2	SWITCH	PUSH-BTN					635800701
S3-7	SWITCH	PUSH-BTN					635800702
S8	SWITCH	PUSH-BTN					635800701
U1-32	DISPLAY	LED-7SEG	0.43"			HI-EFF RED COM ANOD	728301704
U33	DISPLAY	LED-7SEG	0.15"	DIP.12		4-CHAR CNTR DEC	728301705
U34	INT-CKT	LS-TTL	74LS04	DIP.14	P	HEX INVERTER	510907404
U35	INT-CKT	DRIVER	2003	DIP.16	N	7CHN CMOS/TTL INPUT	510075468
XU1-32	SOCKET	PC MOUNT	14 DIL			.300 .255HT TIN	820100600
XU33	SOCKET	W-WRAP	14 DIL			.300 .255HT TIN	820100801

Table DD. Display Driver (A5) Parts List

A2760-00-024
REV 13 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
C1	CAPACITR	ELECT-TA	330 UF	CAP.039	F	6V 20%	310803370
C2-25	CAPACITR	CERAMIC	10 NF	CAP.082	F	16V 20% Y5P	330701031
C26	CAPACITR	CERAMIC	330 PF	CAP.082	N	1KV 10% Z5F	330003310
J1	CABLE	DISP-DRIVER	A				A276000016
J2	CABLE	DISP-DRIVER	B				A276000018
J4	CONNECTR	HEADER	50 DIL			GOLD STRAIGHT	654003311
J5	CONNECTR	HEADER	9 SIL	CONN.1.1		GOLD STRAIGHT	654003427
P6	HARNESS,DISLPAY						A276000065
Q1-16	TRANSSTR	DAR-PNP	MPSU95	TO202.02		40V SI HFE25K 2A	552000095
R1-12	RESISTOR	CARBON	10 K	RES.001	F	1/4W 10%	200101036
R13-15	RESISTOR	CARBON	1.0 K	RES.001	F	1/4W 10%	200101026
R16	RESISTOR	CARBON	10 K	RES.001	F	1/4W 10%	200101036
R17	RESISTOR	CARBON	1.0 K	RES.001	F	1/4W 10%	200101026
R18-26	RESISTOR	CARBON	10 K	RES.001	F	1/4W 10%	200101036
U1-2	INT-CKT	BUF-INVT	8T98	DIP.16	F	HX BUF-INVT DIG	514001203
U3-5	INT-CKT	TTL	8T97	DIP.16	F	HEX BUFFER /3S	514001202
U6	INT-CKT	BUF-INVT	8T98	DIP.16	F	HX BUF-INVT DIG	514001203
U7	INT-CKT	LS-TTL	74LS14	DIP.14	P	HEX SCHMITT TRIGGER	510907414

Table DD. (Cont)

A2760-00-024
REV 13 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
U8	INT-CKT	BUF-INVT	8T98	DIP.16	F	HX BUF-INVT DIG	514001203
U9-10	INT-CKT	TTL	8T97	DIP.16	F	HEX BUFFER /3S	514001202
U11	INT-CKT	TTL	74159	DIP.24.6	N	4-16 DECDR/DMUX/OC	510074159
U12	INT-CKT	LS-TTL	74LS191	DIP.16	P	SYN BINRY U/D CNTR	510974191
U13	INT-CKT	LS-TTL	74LS74	DIP.14	P	2 D POS EDG TRG F-F	510907474
U14	INT-CKT	TTL	7442	DIP.16	N	BCD-DECIMAL DECODER	510074420
U15	INT-CKT	LS-TTL	74LS157	DIP.16	P	4X2IN DATA SEL BUF	510974157
U16	INT-CKT	LS-TTL	74LS156	DIP.16	P	2X2-4 DCDR/DMUX /OC	510974156
U17	INT-CKT	LS-TTL	74LS00	DIP.14	P	4X2 IN NAND GATE	510907400
U18	INT-CKT	LS-TTL	74LS20	DIP.14	P	2X4 IN NAND GATE	510907420
U19	INT-CKT	CMOS	4490	DIP.16	P	HX CNTCT BOUNC ELIM	510004490
U20-25	INT-CKT	RAM-STAT	3101	DIP.16		16X4 5V 60NS	514000402
U26-27	RESISTOR	NETWORK	15X10K	DIP.16		100V 2%	514500101
U28-29	RESISTOR	NETWORK	8X47-R	DIP.16		100V 2%	514500108
U30-31	RESISTOR	NETWORK	8X1K	DIP.16		100V 2%	514500104
W4	CABLE A5.W4 DC						A276000045

Table EE. Interface Board (A6) Parts List

A2760-00-025
REV 14 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
A3.W1	CABLE-A3.W1 DC (INTERCON)						A276000040
C2-4	CAPACITR	ELECT-TA	2.2 UF	CAP.036	F	35V 10%	310002250
C5-13	CAPACITR	CERAMIC	10 NF	CAP.082	F	16V 20% Y5P	330701031
C14	CAPACITR	ELECT-TA	100 NF	CAP.036	F	35V 10%	310001041
J1	HEADER	F-CABLE	50 DIL		P	STR .06PC SHORT L/E	654103050
J2	HEADER	F-CABLE	50 DIL		P	R/A .06PC SHORT L/E	654101050
J3	CONNECTR	HEADER	34 DIL	HDR17.2C		GOLD STRAIGHT	654003319
J4	HEADER	F-CABLE	26 DIL		P	STR .06PC SHORT L/E	654103026
J5	LOCK	FRICTION	2 CKT			RND-WIRE CNTR-WAFR	654003601
J6-9	LOCK	FRICTION	4 CKT			RND-WIRE CNTR-WAFR	654003603
J10-12	LOCK	FRICTION	2 CKT			RND-WIRE CNTR-WAFR	654003601
J13	LOCK	FRICTION	4 CKT			RND-WIRE CNTR-WAFR	654003603
R2	RESISTOR	MTL-FILM	14.3 K	RES.001	N	.25W 1% 100PPM 250V	220214321
R3	RESISTOR	MTL-FILM	20.0 K	RES.001	N	.25W 1% 100PPM 250V	220220021
R4	RESISTOR	CARBON	10 K	RES.001	F	1/4W 10%	200101036
R5	RESISTOR	MTL-FILM	10.0 K	RES.001	P	.25W 1% 100PPM 250V	220210021
R6	RESISTOR	MTL-FILM	1.00 K	RES.001	P	.25W 1% 100PPM 250V	220210011
U1	INT-CKT	MICRO-PR	8212	DIP.24.6		8BT I/O PORT	514001500
U2	INT-CKT	MICRO-PR	8214			PRIORITY INTRPT CON	514001403
U4	INT-CKT	TTL	74393	DIP.14	N	2X4 BINARY RIP CNTR	510074393
U5	INT-CKT	LS-TTL	74LS74	DIP.14	P	2 D POS EDG TRG F-F	510907474
U6	INT-CKT	S-TTL	96S02	DIP.16	N	DUAL ONE SHOT,RETRI	510809602
U7-8	INT-CKT	LS-TTL	74LS155	DIP.16	P	2X2TO4 DECDR/DEMUX	510974155
U9	INT-CKT	LS-TTL	74LS33	DIP.14	P	4X2 IN NOR BUF /OC	510907433
U10	INT-CKT	LS-TTL	74LS21	DIP.14	P	2X4 IN AND GATE	510907421
U11	INT-CKT	LS-TTL	74LS00	DIP.14	P	4X2 IN NAND GATE	510907400
U13-14	INT-CKT	TTL	74390	DIP.16	N	2 DECADE RIP CNTR	510074390
U15	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER	510074040

Table EE. (Cont)

A2760-00-025
REV 14 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
U18-21	INT-CKT	TTL	8T97	DIP.16	F	HEX BUFFER /3S	514001202
U23	INT-CKT	BUF-INVT	8T98	DIP.16	F	HX BUF-INVT DIG	514001203
U24-25	INT-CKT	COMPARTR	339	DIP.14	P	QUAD 5-36V	500000339
U26-27	INT-CKT	TTL	8T97	DIP.16	F	HEX BUFFER /3S	514001202
U28	RESISTOR	NETWORK	15X10K	DIP.16		100V 2%	514500101
U29-30	RESISTOR	NETWORK	8X10K	DIP.16		100V 2%	514500102
U31	INT-CKT	LS-TTL	74LS74	DIP.14	P	2 D POS EDG TRG F-F	510907474
W2	CABLE-PS1 DC						A276000038
XU1-2	SOCKET	PC MOUNT	24 DIL			.600 .180HT GOLD	820101500

Table FF. Accessory Connection Board (A7) Parts List

A2760-00-026
REV 06 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
J3	HEADER	F-CABLE	26 DIL	P	STR .06PC SHORT L/E	654103026
TB1-2	TERMINAL STRIP		9 TERM		BARRIER	850101801

Table GG. 8080 Processor Board (A8) Parts List

A2760-00-032
REV 11 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
W1	CABLE-A8.W1 DC (CPU)	A276000042

Table HH. 8080 Processor Board (A8) Parts List (Component Placement)

A2760-00-066
REV 04 DATED 8/09/84

REFERENCE DESIGNATOR	DESCRIPTION								PART NO.
C1	CAPACITR	ELECT-TA	10	UF	CAP.036	F	10V 10%		310001060
C2	CAPACITR	ELECT-TA	10	UF	CAP.037	F	25V 10%		310001061
C3	CAPACITR	ELECT-TA	10	UF	CAP.036	F	10V 10%		310001060
C4	CAPACITR	ELECT-TA	22	UF	CAP.037	F	15V 10%		310002261
C5	CAPACITR	ELECT-TA	4.7	UF	CAP.036	F	25V 10%		310004751
C6	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V 20%	Y5P	330701031
C7	CAPACITR	ELECT-TA	470	NF	CAP.036	F	50V 10%		310004741
C8-11	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V 20%	Y5P	330701031
C12	CAPACITR	CERAMIC	15	PF	CAP.082	N	1KV 10%	N330	330001500
CR1-4	DIODE	RECTIFER	1N4004		DIO.002		400V SI 1.0A		560040040

Table HH. (Cont)

A2760-00-066
REV 04 DATED 8/09/84

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
J2	HEADER	F-CABLE	50 DIL		P	STR .06PC SHORT L/E	654103050
J3A	CONNECTR	HEADER	8 SIL			R-ANGLE GOLD PC	654003128
J3B	CONNECTR	HEADER	8 SIL			GOLD R-ANGLE	654003228
Q1	TRANSSTR	BJT-PNP	2N6015	TO92.05		60V SI HFE90 800MA	552006015
R1	RESISTOR	CARBON	100 K	RES.001	F	1/4W 10%	200101046
R2	RESISTOR	CARBON	1.0 K	RES.001	F	1/4W 10%	200101026
R3-4	RESISTOR	CARBON	1.5 K	RES.001	F	1/4W 10%	200101526
R5	RESISTOR	CARBON	470 R	RES.001	F	1/4W 10%	200104716
R6-8	RESISTOR	CARBON	1.5 K	RES.001	F	1/4W 10%	200101526
R9	RESISTOR	CARBON	750 R	RES.004	F	1W 10%	200307516
R10	RESISTOR	CARBON	3.3 K	RES.001	F	1/4W 10%	200103326
R11	RESISTOR	CARBON	82 R	RES.001	F	1/4W 10%	200108206
R12	RESISTOR	WIRE-W	700 R	RES.010	N	1W 5%	210107015
R13	RESISTOR	CARBON	560 R	RES.003	F	1/2W 10%	200205616
S2	SWITCH	DIP	5 POS				640001001
S6	SWITCH		SPDT			MOMENTARY PC	635201401
U1	INT-CKT	LS-TTL	74LS74	DIP.14	P	2 D POS EDG TRG F-F	510907474
U2	INT-CKT	LS-TTL	74LS155	DIP.16	P	2X2TO4 DECDR/DEMUX	510974155
U3	INT-CKT	LS-TTL	74LS393	DIP.14	P	2X4BT BIN RIP CNTR	510974393
U4	INT-CKT	TTL	7416	DIP.14	N	HEX INV BUF DRV/OC	510007416
U5	INT-CKT	RECEIVER	1489	DIP.14		QUAD EIA RS-232C	513500301
U6	INT-CKT	LS-TTL	74LS00	DIP.14	P	4X2 IN NAND GATE	510907400
U7	INT-CKT	LS-TTL	74LS125	DIP.14	P	4X3STATE BUS BUFFR	510974125
U8	INT-CKT	LS-TTL	74LS01	DIP.14	P	4X2 IN NAND GT /OC	510907401
U9	INT-CKT	LINE-CKT	9616	DIP.14	N	X3 +/-6V +/- 12PS	510009616
U10	INT-CKT	MICRO-PR	8228			SYS CNTRL BUS DRVR	514001402
U11	INT-CKT	MICRO-PR	8251	DIP.28.6		USART PROG COMM INT	514001602
U12	INT-CKT	LS-TTL	74LS157	DIP.16	P	4X2IN DATA SEL BUF	510974157
U13	INT-CKT	TRANSCVR	1943	DIP.18.3		PROG DUAL RT GEN	514001700
U14	INT-CKT	MICRO-PR	8224	DIP.16		CLOCK GEN/DRIVER	514001401
U15	INT-CKT	MICRO-PR	8080A			NMOS +/-5,12V 8BT	514001400
U16	INT-CKT	LS-TTL	74LS75	DIP.16	P	QUAD BISTBLE LATCH	510907475
U17-19	INT-CKT	LS-TTL	74LS367	DIP.16	P	HEX BUF 2-4BT /3S	510974367
U20	INT-CKT	MICRO-PR	8216			BI-DIR BUS DRIVER	514001404
U21	INT-CKT	LS-TTL	74LS15	DIP.14	P	3X3 IN AND GATE /OC	510907415
U22	INT-CKT	LS-TTL	74LS30	DIP.14	P	8-IN NAND GATE	510907430
U23	INT-CKT	LS-TTL	74LS14	DIP.14	P	HEX SCHMITT TRIGGER	510907414
U24	INT-CKT	MICRO-PR	8216			BI-DIR BUS DRIVER	514001404
U25	INT-CKT	VOLT-REG	7905		N	FIXED NEG 500MA	500003201
U26-27	RESISTOR	NETWORK	7X4.7K	RESNET.8	F	100V 2%	514500001
XU10-11	SOCKET	PC MOUNT	28 DIL		N	.600 .180HT GOLD	820101501
XU13	SOCKET	PC MOUNT	18 DIL		N	.300 .180HT GOLD	820101705
XU14	SOCKET	PC MOUNT	16 DIL		N	.300 .180HT GOLD	820101703
XU15	SOCKET	PC MOUNT	40 DIL		N	.600 .180HT GOLD	820101400
XY1-2	CRYSTAL	INSULATOR					A704000119
Y1	CRYSTAL	FUND-SER	5.0688M	XTAL.001		500PM 32PF 50R HC18	919100009
Y2	CRYSTAL	FUND-PAR	18.000M			50PPM 32PF 500RHC18	919100010

Table II. 4K RAM Board (A9) Parts List

A2760-00-033
REV 08 DATED 5/18/84

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1	CAPACITR ELECT-TA 1.0 UF	CAP.036	F	35V 10%		310001051
C2	CAPACITR CERAMIC 10 NF	CAP.093	F	50V -20 +80% Z5V		330701030
C3	CAPACITR ELECT-TA 1.0 UF	CAP.036	F	35V 10%		310001051
C4	CAPACITR CERAMIC 10 NF	CAP.093	F	50V -20 +80% Z5V		330701030
C5	CAPACITR ELECT-TA 1.0 UF	CAP.036	F	35V 10%		310001051
C6	CAPACITR CERAMIC 10 NF	CAP.093	F	50V -20 +80% Z5V		330701030
C7	CAPACITR ELECT-TA 1.0 UF	CAP.036	F	35V 10%		310001051
C8	CAPACITR CERAMIC 10 NF	CAP.093	F	50V -20 +80% Z5V		330701030
C9	CAPACITR ELECT-TA 22 UF	CAP.036	F	6V 10%		310002260
P2	HEADER F-CABLE 50 DIL		P	STR .06PC SHORT L/E		654103050
R1-4	RESISTOR CARBON 10 K	RES.001	F	1/4W 10%		200101036
U1-32	INT-CKT RAM-STAT 2102A	DIP.16		1KX1 5V 250NS		514000401
U33	INT-CKT LS-TTL 74LS155	DIP.16	P	2X2TO4 DECDR/DEMUX		510974155
U34-35	INT-CKT TRANSCVR 8T26	DIP.16	F	QUAD SNGL-END 3 STA		514001201
U36	INT-CKT TTL 74367	DIP.16	N	HEX BUF 4-2BT /3S		510074367
U37	INT-CKT LS-TTL 74LS27	DIP.14	P	3X3 IN NOR GATE		510907427
U38	INT-CKT LS-TTL 74LS86	DIP.14	P	4X2 IN EXC OR GATE		510907486
W1	CABLE-A9.W1 DC (RAM)					A276000044

Table JJ. ROM RAM Board (A10) Parts List

A2760-00-034
REV 12 DATED 1/10/85

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1	CAPACITR ELECT-TA 10 UF	CAP.037	F	25V 10%		310001061
C2	CAPACITR CERAMIC 10 NF	CAP.082	F	16V 20% Y5P		330701031
C3	CAPACITR ELECT-TA 10 UF	CAP.036	F	10V 10%		310001060
C4	CAPACITR CERAMIC 10 NF	CAP.082	F	16V 20% Y5P		330701031
C5-6	CAPACITR ELECT-TA 1.0 UF	CAP.036	F	35V 10%		310001051
C7-16	CAPACITR CERAMIC 10 NF	CAP.082	F	16V 20% Y5P		330701031
P2	HEADER F-CABLE 50 DIL		P	STR .06PC SHORT L/E		654103050
U1	INT-CKT VOLT-REG 7905	TO220	P	FIXED NEG 1.5A		500079050
U2	INT-CKT TTL 7400	DIP.14	N	4X2 IN NAND GATE		510074000
U3	INT-CKT LS-TTL 74LS367	DIP.16	P	HEX BUF 2-4BT /3S		510974367
U4	INT-CKT LS-TTL 74LS32	DIP.14	P	4X2 IN OR GATE		510907432
U5	INT-CKT LS-TTL 74LS367	DIP.16	P	HEX BUF 2-4BT /3S		510974367
U7	INT-CKT RAM-STAT 2102A	DIP.16	F	1KX1 5V 250NS		514000401
U8	INT-CKT LS-TTL 74LS155	DIP.16	P	2X2TO4 DECDR/DEMUX		510974155
U9	PROM PKG 1-5 MAINFRAME					A276000053
U10	INT-CKT RAM-STAT 2102A	DIP.16	F	1KX1 5V 250NS		514000401
U11	FIRMWARE, 2760 MAINFRAME					A276021801
U12	PROM PKG 1-5 MAINFRAME					A276000053
U13-14	INT-CKT RAM-STAT 2102A	DIP.16	F	1KX1 5V 250NS		514000401
U15	PROM PKG 7 MONITOR					A276000055
U16	PROM PKG 1-5 MAINFRAME					A276000053
U17-18	INT-CKT RAM-STAT 2102A	DIP.16	F	1KX1 5V 250NS		514000401
U19-20	PROM PKG 1-5 MAINFRAME					A276000053
U21-22	INT-CKT RAM-STAT 2102A	DIP.16	F	1KX1 5V 250NS		514000401

Table JJ. (Cont)

ASSEMBLY A2760-00-034
REV 12 DATED 1/10/85

REFERENCE DESIGNATOR	DESCRIPTION		PART NO.
W1	CABLE-A10.W1 DC (ROM)		A276000043
XU9	SOCKET PC MOUNT 24 DIL	.600 .180HT TIN	820101502
XU11-12	SOCKET PC MOUNT 24 DIL	.600 .180HT TIN	820101502
XU15-16	SOCKET PC MOUNT 24 DIL	.600 .180HT TIN	820101502
XU19-20	SOCKET PC MOUNT 24 DIL	.600 .180HT TIN	820101502

Table KK. Power Switch (A19) Parts List

A2760-00-037
REV 06 DATED 1/10/85

REFERENCE DESIGNATOR	DESCRIPTION		PART NO.
F6	CONNECTR HSNG-MAL 6 PIN	MOTOR MOUNT	650800100
S1	SWITCH POWER DPDT	10.5A 250V NEON	630702108

9. GLOSSARY

A. General

9.01 This part defines the terms, abbreviations, and acronyms used in this publication.

ANSWER	Called party goes off-hook.
BACKWARD SIGNALING	Signaling from the terminating end towards the originating end.
BLOCK	16 slots of register signaling memory.
BLOCKED	Interoffice trunk or equipment is busy.
BUSY	The circuit is in use.
CCITT	Consultative Committee on International Telegraph and Telephone.
CLEAR BACKWARD	Called party disconnects (hangs-up).
CLEAR FORWARD	Calling party disconnects (hangs-up).
CODE	A scheme where a digit represents something other than its numerical value.
COMPRESSED DISPLAY	A mode 2 or mode 3 display with brackets [ ] and data between brackets removed. Display is then compressed to fill the space occupied by the deleted data. Applies only to register (address) signaling.
CURSOR	Any visual display indicator which shows a particular character location. In the Model 2760 a blinking digit is used as a cursor. The LDI indicates the digit location in memory.
DIGIT	The numbers 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 are digits.
EDITING	Editing consists of deleting error codes (-), brackets [ ], and data between the brackets.
E-LEAD (SZ1, Sa, SR)	A signaling lead between the trunk circuit and the signaling equipment. Other designations for this lead in worldwide use are shown in parentheses.
ERROR	A received signal with an incorrect number of tones.
FORWARD SIGNALING	Signaling from the originating end towards the terminating end.
GPL	Gap (G) is the interval in milliseconds between two signals. Pulse width (P) is the width or duration of a pulse in milliseconds. Level (L) is the received transmission level of the signal in dBm.
HARD LATCH	A latch condition which may be released only by operator action.
IDLE	To release an interoffice trunk circuit (on-hook condition). Trunk goes idle (on-hook) when released.
INVALID SIGNAL	Signal did not last the minimum time duration.

LATCH	A hold condition.
LDI	LEAD DIGIT IDENT—A three digit display.
LED	Light emitting diode.
LINE SIGNALING	Line signaling indicates the status of a call, e.g. answer, disconnect, etc. Also known as supervision signaling.
METER PULSE	Used to activate billing equipment.
MF	Multifrequency signaling.
MFC	Multifrequency compelled signaling.
M-LEAD (SZ2, Sb, SS)	A signaling lead between the trunk circuit and the signaling equipment. Other designations for this lead in worldwide use are shown in parentheses.
MODE 1	Called number display.
MODE 2	Violation and/or error display.
MODE 3	Measured value display.
MPW	Minimum pulse width.
OFF-HOOK	Interoffice trunk is busy (seized).
ON-HOOK	Interoffice trunk is idle.
PARAMETER	A characteristic such as time between signals, signal transmission level or pulse duration.
PROGRAM ERROR	Two plug-in modules assigned to the same display.
PULSE	A pulse may be a DC pulse, a tone pulse, or a multitone pulse.
REAL TIME	Now, as it occurs.
RECALL	To bring up on the display digits/codes stored in memory.
REGISTER SIGNALING	Register signaling sets up the talking path between two subscribers. Also known as address signaling (called number).
RESET	To release either a hard or soft latch.
REVERSE BATTERY	The battery polarity sent out over an interoffice trunk reverses to indicate an answer condition.
SCROLL	The CURSOR walks through the digits/codes stored in memory.
SEIZURE	To make an interoffice trunk circuit busy (off-hook condition). Trunk goes off-hook when seized.

SEQUENCE MATCH	When the digit/code sequence in a monitored call matches an identical sequence stored in a comparison memory file.
SIGNALING	The transfer of information necessary to establish the talking path and indicate the status of the call.
SLOT	One of the register or supervision memory digit-code locations.
SOFT LATCH	A latch condition which may be released without operator intervention.
SUPERVISION	Signaling pulses which indicate the status of a call.
SUPERVISION EVENT	A change in the status of a call such as answer, disconnect, seizure, etc.
VIOLATION	A signal which violates programmed upper and lower limits for gap, pulse width, or transmission level (GPL).
WILD CARD	A character (c) which will match any digit/code received.
WINK	A signal from the terminating end to the originating end.

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